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2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.

3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

GINSU (K51A)

REFERENCE FROM T18

LAST\_MODIFIED=Thu Feb 19 13:16:29 2009

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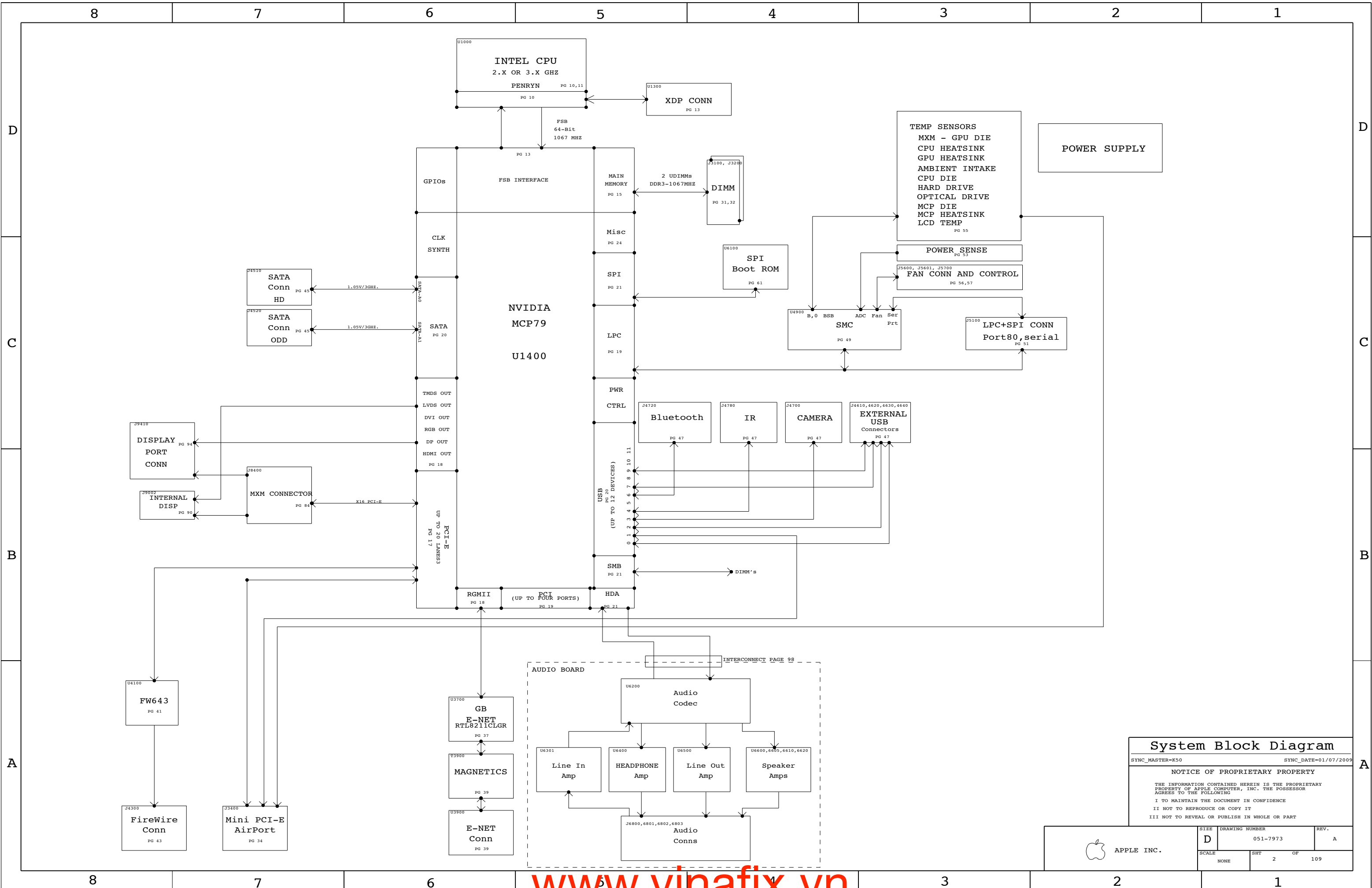
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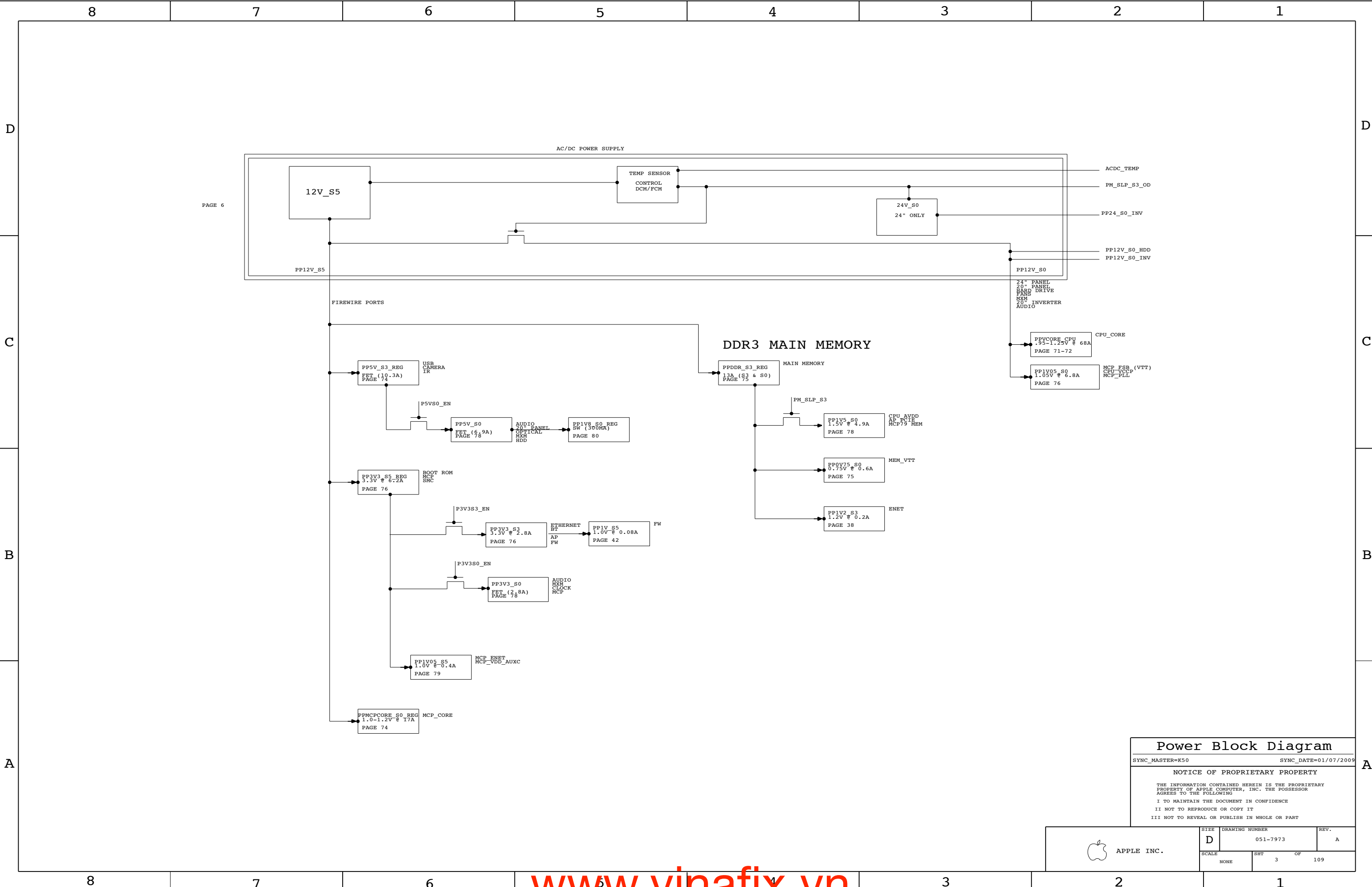
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**Power Block Diagram**

SYNC\_MASTER=K50 SYNC\_DATE=01/07/2009

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APPLE INC.	SIZE D	DRAWING NUMBER 051-7973	REV. A
	SCALE NONE	SHT 3	OF 109

## BOM Variants

## BOM WITH RENASAS FET

BOM NUMBER	BOM NAME	BOM OPTIONS
639-0014	PCBA,MLB,K50A,GOOD,RENESAS FET	20_INCH_LCD,2P66GHZ_CPU,BASIC,IG,RENESAS_FET
607-4701	K50A MLB DEVELOPMENT	DEVELOPMENT,XDP_CONN,LPCPLUS,VREFMRGN,MCP_FWR_SENSE

BOM NUMBER	BOM NAME	BOM OPTIONS
639-0018	PCBA, MLB, K51A, BETTER, RENESAS FET	24_INCH_LCD, 2P66GHZ_CPU, BASIC, IG, RENESAS_FET
639-0019	PCBA, MLB, K51A, BEST, RENESAS FET	24_INCH_LCD, 2P93GHZ_CPU, BASIC, MXM, MXM_PWR_SENSE, 12V_PWR_SENSE, 24_INCH_MXM, RENESAS_FET
639-0020	PCBA, MLB, K51A, CTO_ULT, RENESAS FET	24_INCH_LCD, 3P06GHZ_CPU, BASIC, MXM, MXM_PWR_SENSE, 12V_PWR_SENSE, 24_INCH_MXM, RENESAS_FET
607-4702	K51A MLB DEVELOPMENT	DEVELOPMENT, XDP_CONN, LCPFLS, VREFMRGN, MCP_PWR_SENSE

## BOM WITH TOSHIBA FET

BOM NUMBER	BOM NAME	BOM OPTIONS
639-0013	PCBA,MLB,K50A,GOOD,TOSHIBA FET	20_INCH_LCD,2P66GHZ_CPU,BASIC,IG,TOSHIBA_FET

BOM NUMBER	BOM NAME	BOM OPTIONS
639-0015	PCBA,MLB,K51A,BETTER,TOSHIBA FET	24_INCH_LCD,2P66GHZ_CPU,BASIC,IG,TOSHIBA_FET
639-0016	PCBA,MLB,K51A,BEST,TOSHIBA FET	24_INCH_LCD,2P93GHZ_CPU,BASIC,MMX,MMX_PWR_SENSE,12V_PWR_SENSE,24_INCH_MMX,TOSHIBA_FET
639-0017	PCBA,MLB,K51A,CTO_ULT,TOSHIBA FET	24_INCH_LCD,3P06GHZ_CPU,BASIC,MMX,MMX_PWR_SENSE,12V_PWR_SENSE,24_INCH_MMX,TOSHIBA_FET

## BOM GROUPS

BOM GROUP	BOM OPTIONS
BASIC	COMMON,ALTERNATE,MCP_TDIODE,MCP79,CPUV_PHASE3,XDP,CPU_TDIODE,MCP_B02,PRODUCTION
MCP79	BOOT_MODE_USER,MEMRESET_HW,MEMRESET_MCP

## CPUS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S3705	1	1C, PRQ,FDC, SLGED, 2.66, 55W, 1066, 0E, 68, PGA	CPU	CRITICAL	2P66GZH_CPU
337S3706	1	1C, PRQ,FDC, SLGEB, 2.93, 55W, 1066, 0E, 68, PGA	CPU	CRITICAL	2P93GZH_CPU
337S3707	1	1C, PRQ,FDC, SLGEA, 3.06, 55W, 1066, 0E, 68, PGA	CPU	CRITICAL	3P06GZH_CPU

## BOARD STACK-UP

TOP	SIGNAL
2	GROUND
3	SIGNAL
4	POWER
5	POWER
6	SIGNAL
7	GROUND
BOTTOM	SIGNAL

COMMON (DELETED HDCP ROM)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0636	1	IC_OMCF_MCP79-B02,35X35MM, BGA1437, DT	U1400	CRITICAL	MCP_B02
338S0654	1	IC_FW643-06,1394B, REV-E	U4100	CRITICAL	
820-2404	1	PCB,FAB,IO ALIGNMENT,K50/K51	IO1	CRITICAL	
825-7122	1	MLB LABEL,48.0X4.8	X14	CRITICAL	
341T0174	1	EFI ROM,K50A/K51A/K50E	U6100	CRITICAL	
511S0038	1	CONN,INTEL SKT-P, BGA,26X26-479	U1000	CRITICAL	
338S0570	1	IC_RTL8211CGL,GIGE TRANSCEIVER, 48P TQFP	U3700	CRITICAL	

## K50A PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-7972	1	PCB,SCHM,MLB,K50A	SCH1		20_INCH_LCD
820-2347	1	PCB,FAB,MLB,K50,HF	MLB1		20_INCH_LCD
341T0173	1	IC,SMC,K50A/K50E	U4900	CRITICAL	20_INCH_LCD
11480305	1	RES,7.87K,0402,1%,1/16W,LF	R7117		20_INCH_LCD
132S0201	1	CAP,CER,270PF,10%,50V,0402	C7113		20_INCH_LCD
132S0178	1	CAP,CER,0.47UF,10%,6.3V,0402	C7128		20_INCH_LCD
132S0082	1	CAP,CER,0.068UF,10%,10V,0402	C7134		20_INCH_LCD

## K51A PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-7973	1	PCB,SCHEN,MLB,K51A	SCH1		24_INCH_LCD
820-2491	1	PCB,FAB,MLB,K51,HF	MLB1		24_INCH_LCD
341T0177	1	IC,SMC,K51A	U4900	CRITICAL	24_INCH_LCD
114S0308	1	RES,8.45K,0402,18,1/16W,LF	R7117		24_INCH_LCD
132S0010	1	CAP,CER,390PF,108,50V,0402	C7113		24_INCH_LCD
132S0178	1	CAP,CER,0.47UF,108,6.3V,0402	C7128		24_INCH_LCD
132S0082	1	CAP,CER,0.068UF,108,10V,0402	C7134		24_INCH_LCD

## ALTERNATES

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152-0104	152-0099		L100,L7101,L200	MSQ-1211-R36L-F
152-0105	152-0101		L7530	MSQ-1211-1R5L-F
33850694	33850570		U3760	RTL8211CL/RTL8251CA
10450018	10150410		R5400	USE 20MHZ AS OR

## BOM Configuration

SYNC_MASTER=K50A	SYNC_DATE=01/13/2009
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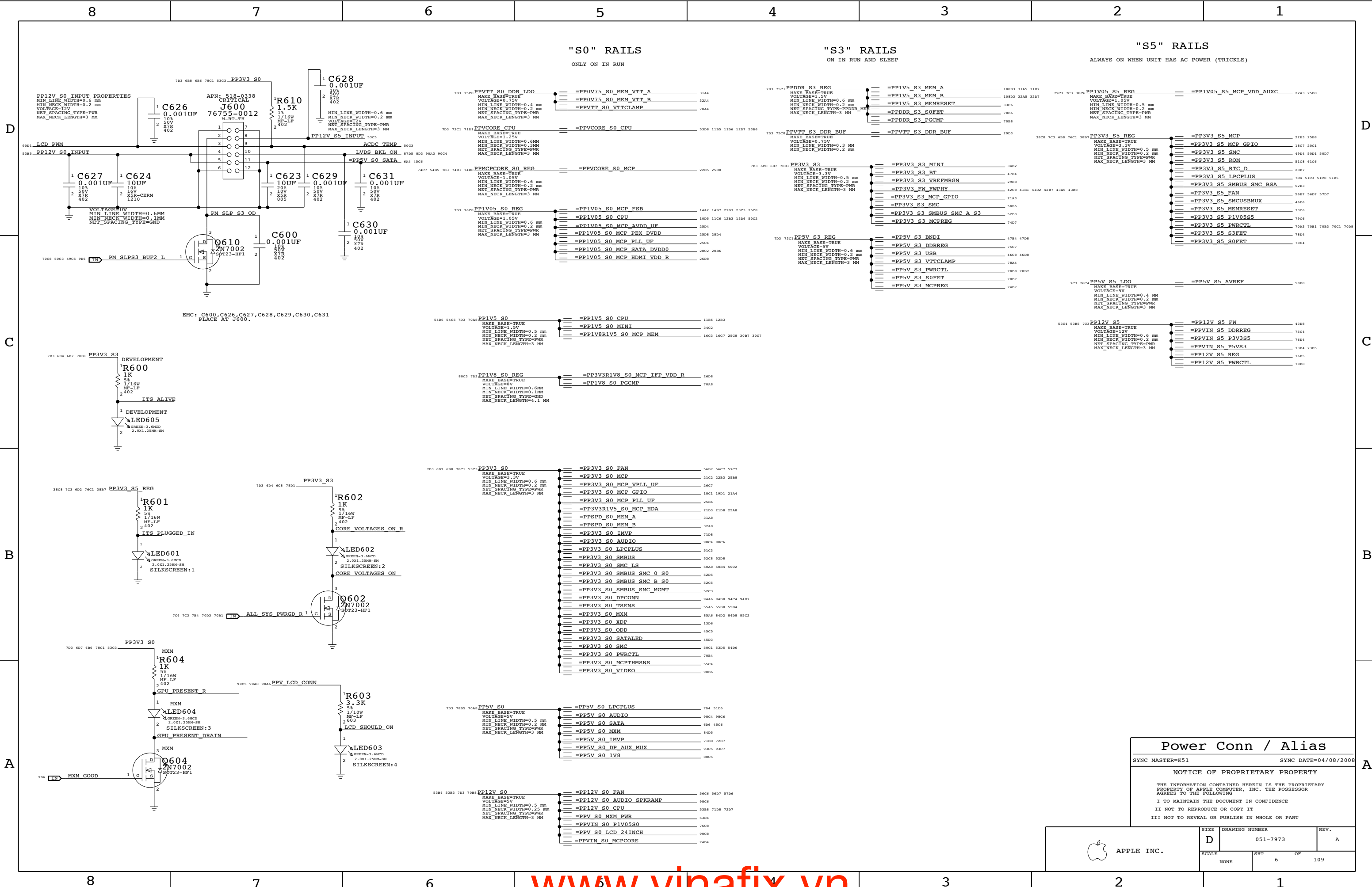
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	SCALE	SHT OF	
	NONE	4 109	

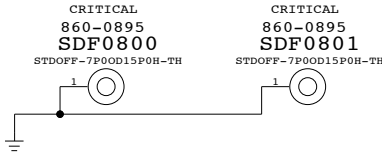


Power Conn / Alias		
SYNC_MASTER=K51		SYNC_DATE=04/08/2008
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	SCALE NONE	SHT 6	OF 109





8		7		6		5		4		3		2		1									
D	NC ON UNUSED ALIASES														D								
	18C6	MCP_TV_DAC_RSET	=	NC_MCP_TV_DAC_RSET	MAKE_BASE=TRUE	NO_TEST=TRUE	18C6	TP_ENET_INTR_L	=	NC_ENET_INTR_L	MAKE_BASE=TRUE	NO_TEST=TRUE	1786	PCIE_EXCARD_D2R_P		=	TP_PCIE_EXCARD_D2R_P	MAKE_BASE=TRUE					
	18C6	MCP_TV_DAC_VREF	=	NC_MCP_TV_DAC_VREF	MAKE_BASE=TRUE	NO_TEST=TRUE	18C3	TP_ENET_PWRDWN_L	=	NC_ENET_PWDWN_L	MAKE_BASE=TRUE	NO_TEST=TRUE	1786	PCIE_EXCARD_D2R_N		=	TP_PCIE_EXCARD_D2R_N	MAKE_BASE=TRUE					
	18C6	MCP_CLK27M_XTALIN	=	NC_MCP_CLK27M_XTALIN	MAKE_BASE=TRUE	NO_TEST=TRUE	21C7	TP_MCP_KBDRSTIN_L	=	NC_MCP_KBDRSTIN_L	MAKE_BASE=TRUE	NO_TEST=TRUE	1783	PCIE_EXCARD_R2D_C_P		=	TP_PCIE_EXCARD_R2D_C_P	MAKE_BASE=TRUE					
	18C6	MCP_CLK27M_XTALOUT	=	NC_MCP_CLK27M_XTALOUT	MAKE_BASE=TRUE	NO_TEST=TRUE	1786	TP_MCP_GPIO_18	=	NC_MCP_GPIO_18	MAKE_BASE=TRUE	NO_TEST=TRUE	1783	PCIE_EXCARD_R2D_C_N		=	TP_PCIE_EXCARD_R2D_C_N	MAKE_BASE=TRUE					
	18C3	CRT_IG_R_C_PR	=	NC_CRT_IG_R_C_PR	MAKE_BASE=TRUE	NO_TEST=TRUE	21D7	TP_MLB_RAM_SIZE	=	NC_MLB_RAM_SIZE	MAKE_BASE=TRUE	NO_TEST=TRUE	71C7	VR_PWRGD_CLKEN_L		=	TP_VR_PWRGD_CLKEN_L	MAKE_BASE=TRUE					
	18C3	CRT_IG_G_Y_Y	=	NC_CRT_IG_G_Y_Y	MAKE_BASE=TRUE	NO_TEST=TRUE	19D4	TP_PCI_C_BE_L<3>	=	NC_PCI_C_BE_L<3>	MAKE_BASE=TRUE	NO_TEST=TRUE	90C4 90A3 6D6 87D5 <b>NEW</b> LVDS_BKL_ON										
	18C3	CRT_IG_B_COMP_PB	=	NC_CRT_IG_B_COMP_PB	MAKE_BASE=TRUE	NO_TEST=TRUE	19C4	TP_PCI_CLK0	=	NC_PCI_CLK0	MAKE_BASE=TRUE	NO_TEST=TRUE	MAKE_BASE=TRUE										
	18C3	CRT_IG_HSYNC	=	NC_CRT_IG_HSYNC	MAKE_BASE=TRUE	NO_TEST=TRUE	19C4	TP_PCI_CLK1	=	NC_PCI_CLK1	MAKE_BASE=TRUE	NO_TEST=TRUE	UNUSED INTERNAL USB PORTS										
	18C3	CRT_IG_VSYNC	=	NC_CRT_IG_VSYNC	MAKE_BASE=TRUE	NO_TEST=TRUE	19D4	TP_PCI_FRAME_L	=	NC_PCI_FRAME_L	MAKE_BASE=TRUE	NO_TEST=TRUE											
	18C3	TP_MCP_RGB_HSYNC	=	NC_MCP_RGB_HSYNC	MAKE_BASE=TRUE	NO_TEST=TRUE	19D4	TP_PCI_GNT0_L	=	NC_MCP_PCI_GNT0_L	MAKE_BASE=TRUE	NO_TEST=TRUE											
	18C3	TP_MCP_RGB_VSYNC	=	NC_MCP_RGB_VSYNC	MAKE_BASE=TRUE	NO_TEST=TRUE	19D4	TP_PCI_GNT1_L	=	NC_PCI_GNT1_L	MAKE_BASE=TRUE	NO_TEST=TRUE											
	19C7	TP_PCI_AD<31..15>	=	NC_PCI_AD<31..15>	MAKE_BASE=TRUE	NO_TEST=TRUE	19C7	TP_PCI_INTW_L	=	NC_PCI_INTW_L	MAKE_BASE=TRUE	NO_TEST=TRUE											
	19D4	TP_PCI_IRDY_L	=	NC_PCI_IRDY_L	MAKE_BASE=TRUE	NO_TEST=TRUE	19C7	TP_PCI_INTX_L	=	NC_PCI_INTX_L	MAKE_BASE=TRUE	NO_TEST=TRUE											
	19D4	TP_PCI_C_BE_L<1..0>	=	NC_PCI_C_BE_L<1..0>	MAKE_BASE=TRUE	NO_TEST=TRUE	19C7	TP_PCI_INTY_L	=	NC_PCI_INTY_L	MAKE_BASE=TRUE	NO_TEST=TRUE											
	19D4	TP_PCI_SERR_L	=	NC_PCI_SERR_L	MAKE_BASE=TRUE	NO_TEST=TRUE	19C7	TP_PCI_INTZ_L	=	NC_PCI_INTZ_L	MAKE_BASE=TRUE	NO_TEST=TRUE											
	19D4	TP_PCI_DEVSEL_L	=	NC_PCI_DEVSEL_L	MAKE_BASE=TRUE	NO_TEST=TRUE	19D4	TP_PCI_PAR	=	NC_PCI_PAR	MAKE_BASE=TRUE	NO_TEST=TRUE											
19D4	TP_PCI_PERR_L	=	NC_PCI_PERR_L	MAKE_BASE=TRUE	NO_TEST=TRUE	19C4	TP_PCI_RESET1_L	=	NC_PCI_RESET1_L	MAKE_BASE=TRUE	NO_TEST=TRUE												
1987	TP_LPC_DRQ0_L	=	NC_LPC_DRQ0_L	MAKE_BASE=TRUE	NO_TEST=TRUE	19D4	TP_PCI_STOP_L	=	NC_PCI_STOP_L	MAKE_BASE=TRUE	NO_TEST=TRUE												
21B3	TP_MCP_BUF_SIO_CLK	=	NC_MCP_BUF_SIO_CLK	MAKE_BASE=TRUE	NO_TEST=TRUE	19C7	TP_PCI_TRDY_L	=	NC_PCI_TRDY_L	MAKE_BASE=TRUE	NO_TEST=TRUE												
16D6	TP_MEM_A_ODT<3..2>	=	NC_MEM_A_ODT<3..2>	MAKE_BASE=TRUE	NO_TEST=TRUE	17C3	TP_PCIE_CLK100M_PE4N	=	NC_PCIE_CLK100M_PE4N	MAKE_BASE=TRUE	NO_TEST=TRUE												
16D6	TP_MEM_A_CKE<3..2>	=	NC_MEM_A_CKE<3..2>	MAKE_BASE=TRUE	NO_TEST=TRUE	17C3	TP_PCIE_CLK100M_PE4P	=	NC_PCIE_CLK100M_PE4P	MAKE_BASE=TRUE	NO_TEST=TRUE												
16D6	TP_MEM_A_CS_L<3..2>	=	NC_MEM_A_CS_L<3..2>	MAKE_BASE=TRUE	NO_TEST=TRUE	1783	TP_PCIE_CLK100M_PE5N	=	NC_PCIE_CLK100M_PE5N	MAKE_BASE=TRUE	NO_TEST=TRUE												
1585	TP_MEM_A_CLK2P	=	NC_MEM_A_CLK2P	MAKE_BASE=TRUE	NO_TEST=TRUE	1783	TP_PCIE_CLK100M_PE5P	=	NC_PCIE_CLK100M_PE5P	MAKE_BASE=TRUE	NO_TEST=TRUE												
1585	TP_MEM_A_CLK2N	=	NC_MEM_A_CLK2N	MAKE_BASE=TRUE	NO_TEST=TRUE	1783	TP_PCIE_CLK100M_PE6P	=	NC_PCIE_CLK100M_PE6P	MAKE_BASE=TRUE	NO_TEST=TRUE												
16D6	TP_MEM_A_CLK3P	=	NC_MEM_A_CLK3P	MAKE_BASE=TRUE	NO_TEST=TRUE	17C6	PCIE_EXCARD_PRSNT_L	=	NC_PCIE_EXCARD_PRSNT_L	MAKE_BASE=TRUE	NO_TEST=TRUE												
16D6	TP_MEM_A_CLK3N	=	NC_MEM_A_CLK3N	MAKE_BASE=TRUE	NO_TEST=TRUE	17C6	TP_PE4_CLKREQ_L	=	NC_PE4_CLKREQ_L	MAKE_BASE=TRUE	NO_TEST=TRUE												
16D6	TP_MEM_A_CLK4P	=	NC_MEM_A_CLK4P	MAKE_BASE=TRUE	NO_TEST=TRUE	17C6	TP_PE4_PRSNT_L	=	NC_PE4_PRSNT_L	MAKE_BASE=TRUE	NO_TEST=TRUE												
16D6	TP_MEM_A_CLK4N	=	NC_MEM_A_CLK4N	MAKE_BASE=TRUE	NO_TEST=TRUE	21C7	TP_SB_A20GATE	=	NC_SB_A20GATE	MAKE_BASE=TRUE	NO_TEST=TRUE												
16D6	TP_MEM_A_CLK5P	=	NC_MEM_A_CLK5P	MAKE_BASE=TRUE	NO_TEST=TRUE	20C3	TP_USB_10N	=	NC_USB_10N	MAKE_BASE=TRUE	NO_TEST=TRUE												
16D6	TP_MEM_A_CLK5N	=	NC_MEM_A_CLK5N	MAKE_BASE=TRUE	NO_TEST=TRUE	20C3	TP_USB_10P	=	NC_USB_10P	MAKE_BASE=TRUE	NO_TEST=TRUE												
16D3	TP_MEM_B_CS_L<3..2>	=	NC_MEM_B_CS_L<3..2>	MAKE_BASE=TRUE	NO_TEST=TRUE	20C3	TP_USB_11N	=	NC_USB_11N	MAKE_BASE=TRUE	NO_TEST=TRUE												
16D3	TP_MEM_B_ODT<3..2>	=	NC_MEM_B_ODT<3..2>	MAKE_BASE=TRUE	NO_TEST=TRUE	20C3	TP_USB_11P	=	NC_USB_11P	MAKE_BASE=TRUE	NO_TEST=TRUE												
16D3	TP_MEM_B_CKE<3..2>	=	NC_MEM_B_CKE<3..2>	MAKE_BASE=TRUE	NO_TEST=TRUE	20C3	USB_EXCARD_N	=	NC_USB_EXCARD_N	MAKE_BASE=TRUE	NO_TEST=TRUE												
1581	TP_MEM_B_CLK2P	=	NC_MEM_B_CLK2P	MAKE_BASE=TRUE	NO_TEST=TRUE	20C3	USB_EXCARD_P	=	NC_USB_EXCARD_P	MAKE_BASE=TRUE	NO_TEST=TRUE												
1581	TP_MEM_B_CLK2N	=	NC_MEM_B_CLK2N	MAKE_BASE=TRUE	NO_TEST=TRUE	21B3	ODD_PWR_EN_L	=	NC_ODD_PWR_EN_L	MAKE_BASE=TRUE	NO_TEST=TRUE												
16D3	TP_MEM_B_CLK3P	=	NC_MEM_B_CLK3P	MAKE_BASE=TRUE	NO_TEST=TRUE	17C3	PCIE_CLK100M_EXCARD_P	=	NC_PCIE_CLK100M_EXCARD_P	MAKE_BASE=TRUE	NO_TEST=TRUE												
16D3	TP_MEM_B_CLK3N	=	NC_MEM_B_CLK3N	MAKE_BASE=TRUE	NO_TEST=TRUE	17C3	PCIE_CLK100M_EXCARD_N	=	NC_PCIE_CLK100M_EXCARD_N	MAKE_BASE=TRUE	NO_TEST=TRUE												
16D3	TP_MEM_B_CLK4P	=	NC_MEM_B_CLK4P	MAKE_BASE=TRUE	NO_TEST=TRUE	17C6	EXCARD_CLKREQ_L	=	NC_EXCARD_CLKREQ_L	MAKE_BASE=TRUE	NO_TEST=TRUE												
16D3	TP_MEM_B_CLK4N	=	NC_MEM_B_CLK4N	MAKE_BASE=TRUE	NO_TEST=TRUE	19D7	TP_PCI_AD<12..10>	=	NC_PCI_AD<12..10>	MAKE_BASE=TRUE	NO_TEST=TRUE												
16D3	TP_MEM_B_CLK5P	=	NC_MEM_B_CLK5P	MAKE_BASE=TRUE	NO_TEST=TRUE	19D7	TP_PCI_AD<8>	=	NC_PCI_AD<8>	MAKE_BASE=TRUE	NO_TEST=TRUE												
16D3	TP_MEM_B_CLK5N	=	NC_MEM_B_CLK5N	MAKE_BASE=TRUE	NO_TEST=TRUE	TESTPOINT FOR OPTIONAL GMUX JTAG FROM MCP																	
K51 ONLY STANDOFFS																							
																							
UNUSED SIGNAL ALIAS/STAND OFF																							
SYNC_MASTER=K51 SYNC_DATE=04/07/2008																							
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```

1080 CPU_PSI_L == IMVP6_PSI_L 7107
== MAKE_BASE=TRUE

2107 TP_MLB_RAM_VENDOR == MXM_GOOD 6A8
== MAKE_BASE=TRUE

```

The schematic diagram illustrates the power plane connections. At the top, two signal lines are shown: **1080 CPU\_PSI\_L** and **2107 TP\_MLB\_RAM\_VENDOR**. The **1080 CPU\_PSI\_L** line is connected to **IMVP6\_PSI\_L** (pin 7107) via a **MAKE\_BASE=TRUE** connection. The **2107 TP\_MLB\_RAM\_VENDOR** line is connected to **MXM\_GOOD** (pin 6A8) via a **MAKE\_BASE=TRUE** connection. Below these, a network of components is shown. A resistor **R910** (15 ohms, 1/16W, NP-LF, 402) is connected between the **1080 CPU\_PSI\_L** line and a node labeled **PM\_SLP33 BUF2\_L**. This node is also connected to a capacitor **C1** (1000pF, 50V, NP-LF, 402) and an inductor **L1** (100nH, 50V, NP-LF, 402). The **PM\_SLP33 BUF2\_L** line is connected to **MAKE\_BASE=TRUE** and has a note: **(P50 HAS A 100K TO GROUND)**. Another resistor **R911** (15 ohms, 1/16W, NP-LF, 402) is connected between the **1080 CPU\_PSI\_L** line and a node labeled **PM\_SLP33 BUF1\_L**. This node is also connected to a capacitor **C2** (1000pF, 50V, NP-LF, 402) and an inductor **L2** (100nH, 50V, NP-LF, 402). The **PM\_SLP33 BUF1\_L** line is connected to **MAKE\_BASE=TRUE** and has a note: **(P50 HAS A 100K TO GROUND)**. A resistor **R912** (100K, 50V, NP-LF, 402) is connected between the **PM\_SLP33 BUF1\_L** line and ground. The ground symbol is shown at the bottom of the diagram.

1703	1R	PEG_CLK100M_P	=	GPU_CLK100M_PCIE_P	GPU	87C5	102C3
				MAKE_BASE=TRUE			
1703	1R	PEG_CLK100M_N	=	GPU_CLK100M_PCIE_N	GPU	87C5	102C3 7C3
				MAKE_BASE=TRUE			
1703 1703	1R	=PEG_R2D_C P<0..15>	=	PEG_R2D_C P<0..15>	GPU	102D3 86A7 86B7 86C7 86D7	
				MAKE_BASE=TRUE			
1703 1703	1R	=PEG_R2D_C N<0..15>	=	PEG_R2D_C N<0..15>	GPU	102D3 86A7 86B7 86C7 86D7	
				MAKE_BASE=TRUE			
1706 1706	00W	=PEG_D2R_P<0..15>	=	PEG_D2R_P<0..15>	GPU	78B7 86A1 86B1 86C1 86D1 102D3	
				MAKE_BASE=TRUE			
1706 1706	00W	=PEG_D2R_N<0..15>	=	PEG_D2R_N<0..15>	GPU	78B7 86A1 86A1 86C1 86D1 102D3	
				MAKE_BASE=TRUE			
1706	1R	PEG_PRSNT_L	=	MMX_DETECT_L	GPU	85B6 85B3	
				MAKE_BASE=TRUE			

1886A	IN	=MCP_HDMI_TXC_P	DP_IG_ML_P<3>	0000	107D2	91C4
		MAKE_BASE=TRUE				
1886B	IN	=MCP_HDMI_TXC_N	DP_IG_ML_N<3>	0000	107D2	91D4
		MAKE_BASE=TRUE				
1886C	IN	=MCP_HDMI_TXD_P<0..2>	DP_IG_ML_P<2..0>	0000	107D2	91B7 91B8 91CB
		MAKE_BASE=TRUE				
1886D	IN	=MCP_HDMI_TXD_N<0..2>	DP_IG_ML_N<2..0>	0000	107D2	91B8 91CB 91D8
		MAKE_BASE=TRUE				
18A3	IN	=MCP_HDMI_DDC_CLK	DP_IG_DDC_CLK	0000	93CB	
		MAKE_BASE=TRUE				
18A7	BT	=MCP_HDMI_DDC_DATA	DP_IG_DDC_DATA	0000	93CB	91D8
		MAKE_BASE=TRUE				
18B0	OUT	=MCP_HDMI_HPD	DP_IG_HPD	AN	91B4	
		MAKE_BASE=TRUE				

18B6 =DVI\_HPD\_GMUX\_INT= HPLUG\_DET2 MAKE\_BASE=TRUE

1 2

20K

5%

1/16W

MS-LF

402

CP79 PCIe PRSNT# Str

PCIE\_FW\_PRSNT\_L 17C6

PCIE\_MINI\_PRSNT\_L 17C6

The image displays a PCB layout with several components and a large ground area. At the top, there are labels for 'PGOOD\_5V\_S3', 'PM\_EN\_USB\_PWR', and 'GND'. Below these, the text 'GROUND ALIAS' and 'GND RAILS' is prominently displayed. On the left, there is a label '980d GND\_AUDIO\_SPKRAMP'. On the right, there is a label 'GND' with associated parameters: 'MIN\_LINE\_WIDTH=0.6 mm', 'MIN\_NECK\_WIDTH=0.09mm', 'VOLTAGE=5V', 'NET\_SPACING\_TYPE=GND', 'MAKE\_BASE=TRUE', and 'MAX\_NECK\_LENGTH=4.1 mm'. The layout includes various traces, pads, and a large ground plane area.

103D3 19C3 **LR** **LPC RESET L**

PLACEMENT\_NOTE=Place close to U1400

**R981**  
33  
1 2  
5V  
1/16W  
NF-LF  
402

**DEBUG RESET L** **Q9P** 7D4 51D5

**R983**  
33  
1 2  
5V  
1/16W  
NF-LF  
402

**SMC LRESET L** **Q9P** 7D6 49C8

PLACEMENT\_NOTE=Place close to U1400

1701 **IN** PCIE\_RESET\_L

R992  
0  
5k  
1/16W  
MF-LF  
402

FW\_RESET\_L **OUT** 706 783 41A2

R991  
0  
5k  
1/16W  
MF-LF  
402

MINI\_RESET\_L **OUT** 14C3

R990  
0  
5k  
1/16W  
MF-LF  
402

PEG\_RESET\_L **OUT** 67C5 90D4

R971  
0  
5k  
1/16W  
MF-LF  
402

PCA9557D\_RESET\_L **OUT** 29A5

10C4 **IN** MEM\_VTT\_EN\_R

R972  
33  
5k  
1/16W  
MF-LF  
402

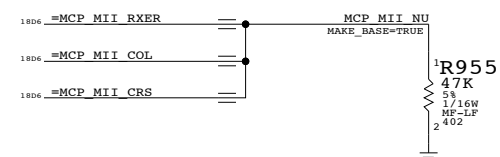
DDR\_VTT\_EN **OUT** 75C8 78A4

NO STUFF  
C973  
0.47UF  
10%  
6.3V  
CERM-X5R  
402

2183 MCP\_CPUVDD\_EN 1 2 2 R930 22 2 MCP\_CPU\_VLD 2187

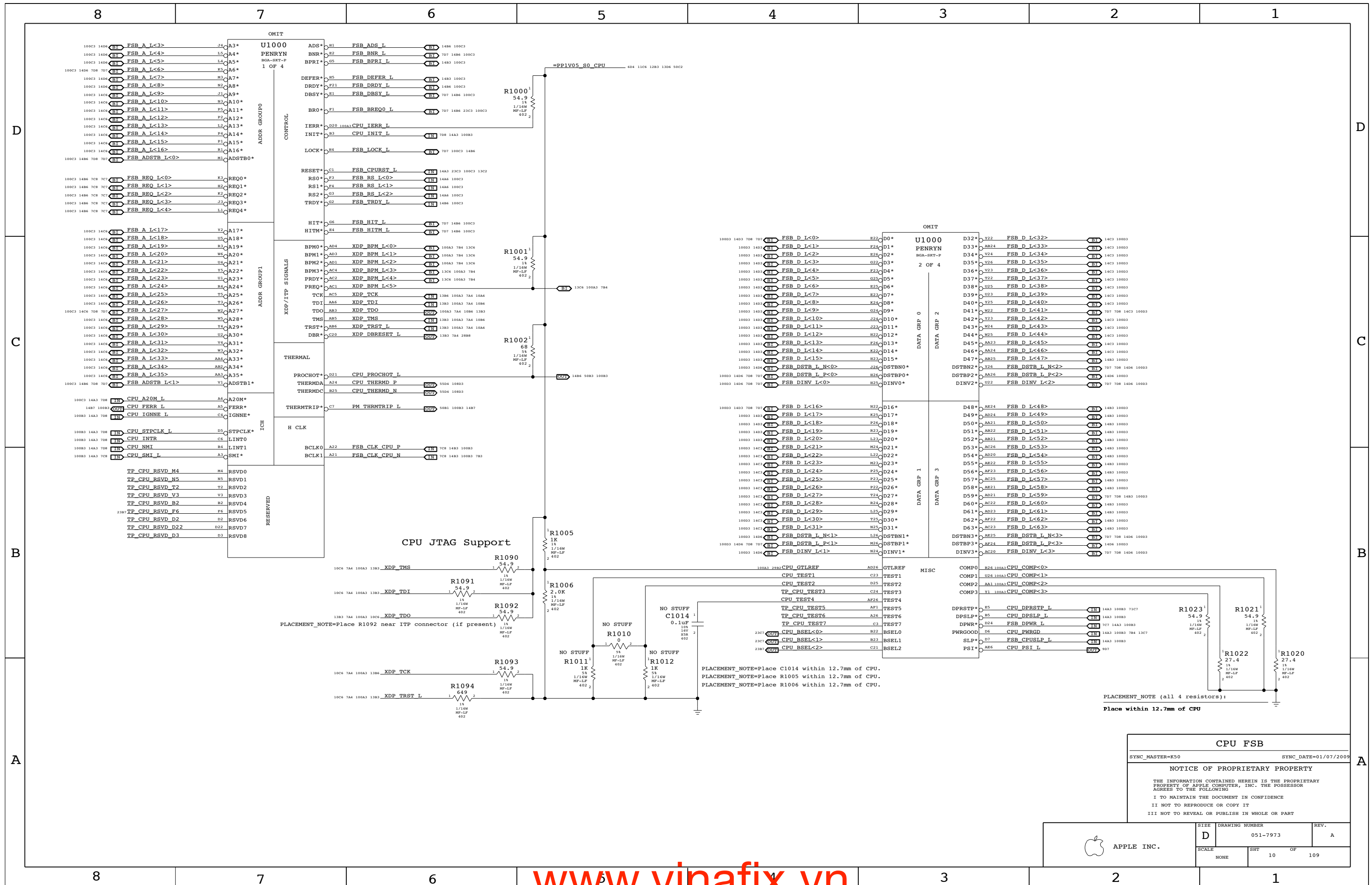
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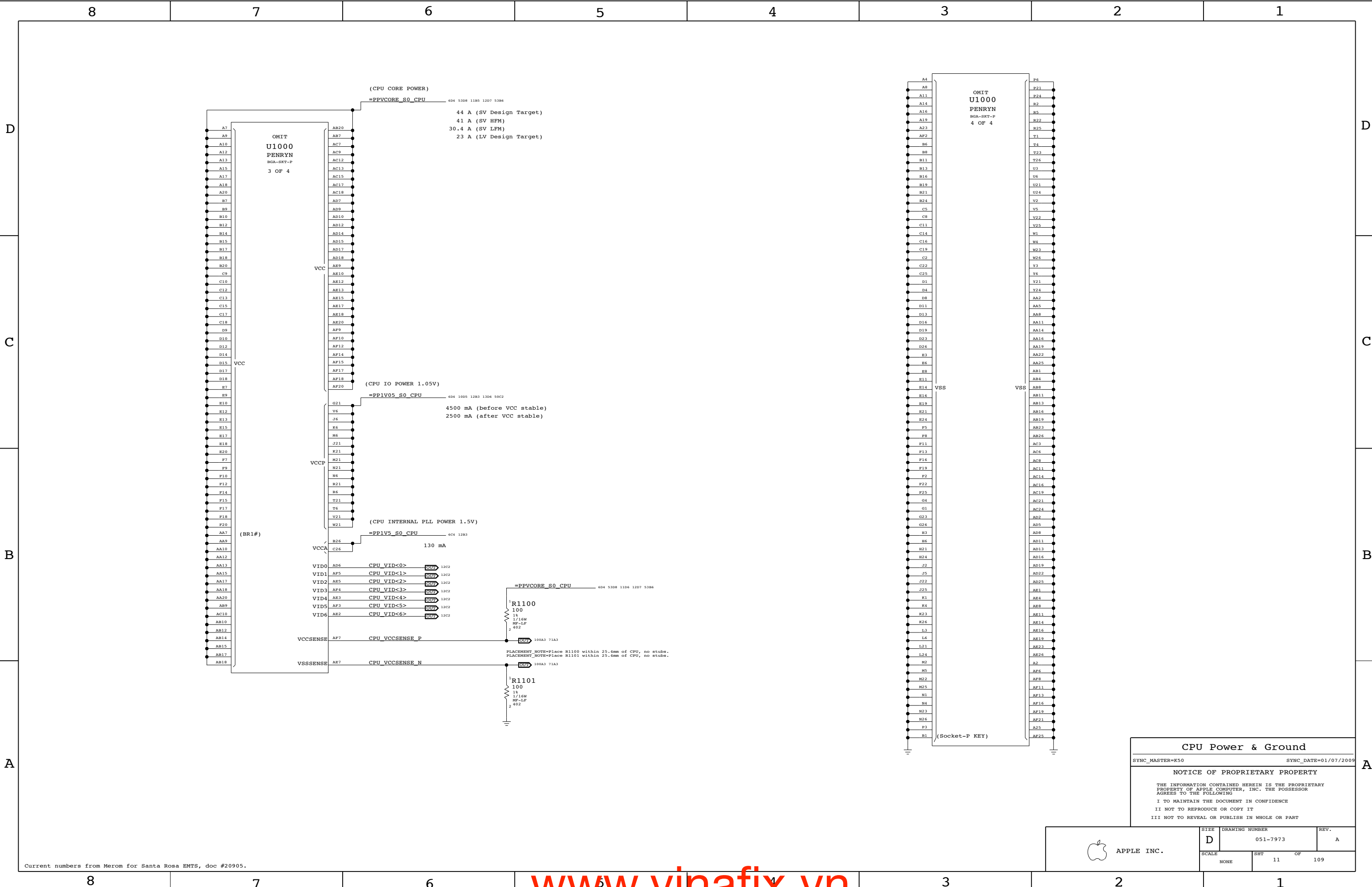
1/16W  
MF-LF  
402



<h1 style="text-align: center;">SIGNAL &amp; GND ALIASES</h1>			
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		<div> <div>REV.</div> <div>A</div> </div>	
<div> <div>SCALE</div> <div>NONE</div> </div>		<div> <div>SHT</div> <div>9</div> </div>	
		<div> <div>OF</div> <div>109</div> </div>	







Current numbers from Merom for Santa Rosa EMTS, doc #20905.

CPU Power & Ground

SYNC\_MASTER=K50

SYNC\_DATE=01/07/2009

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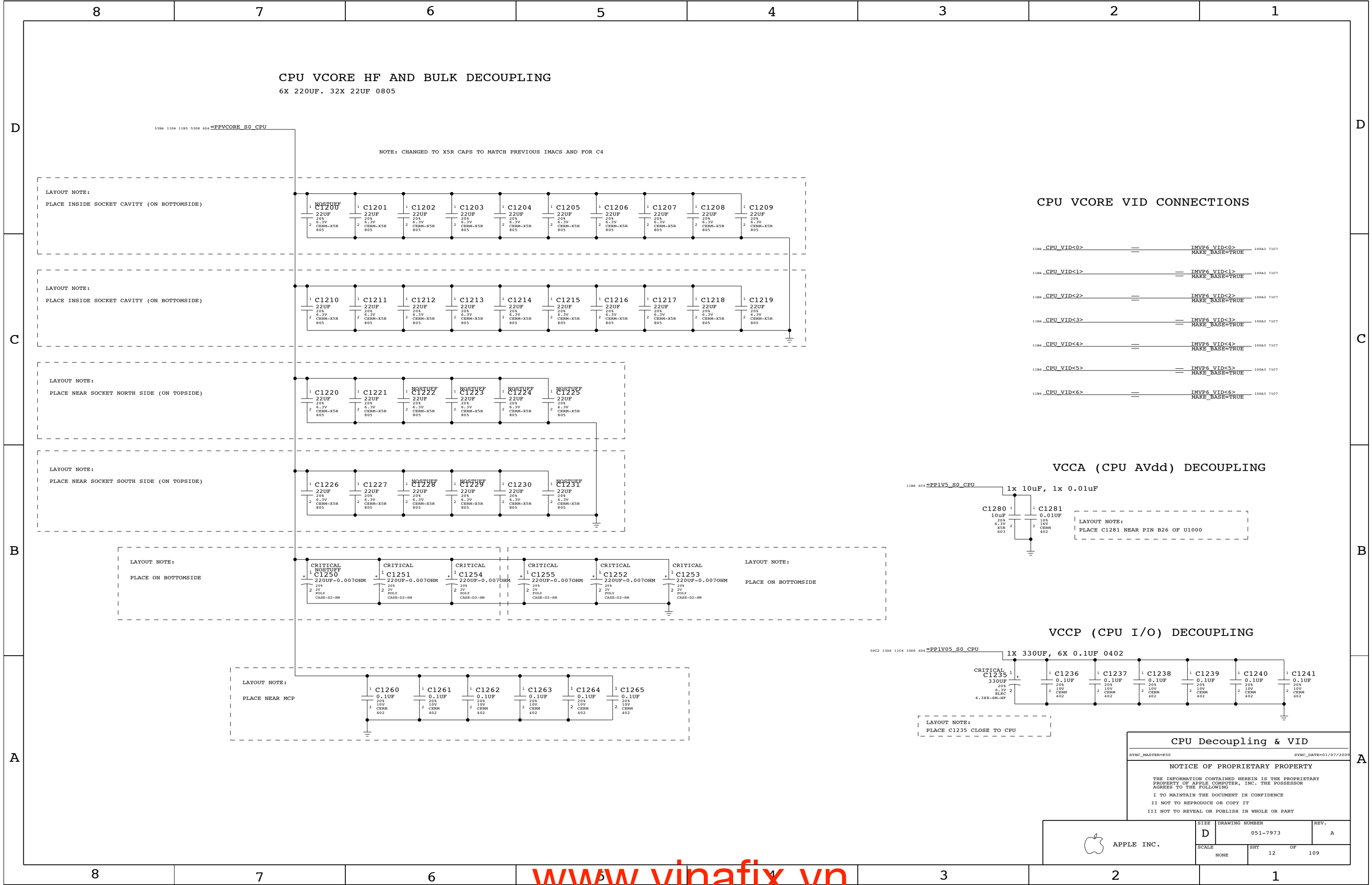
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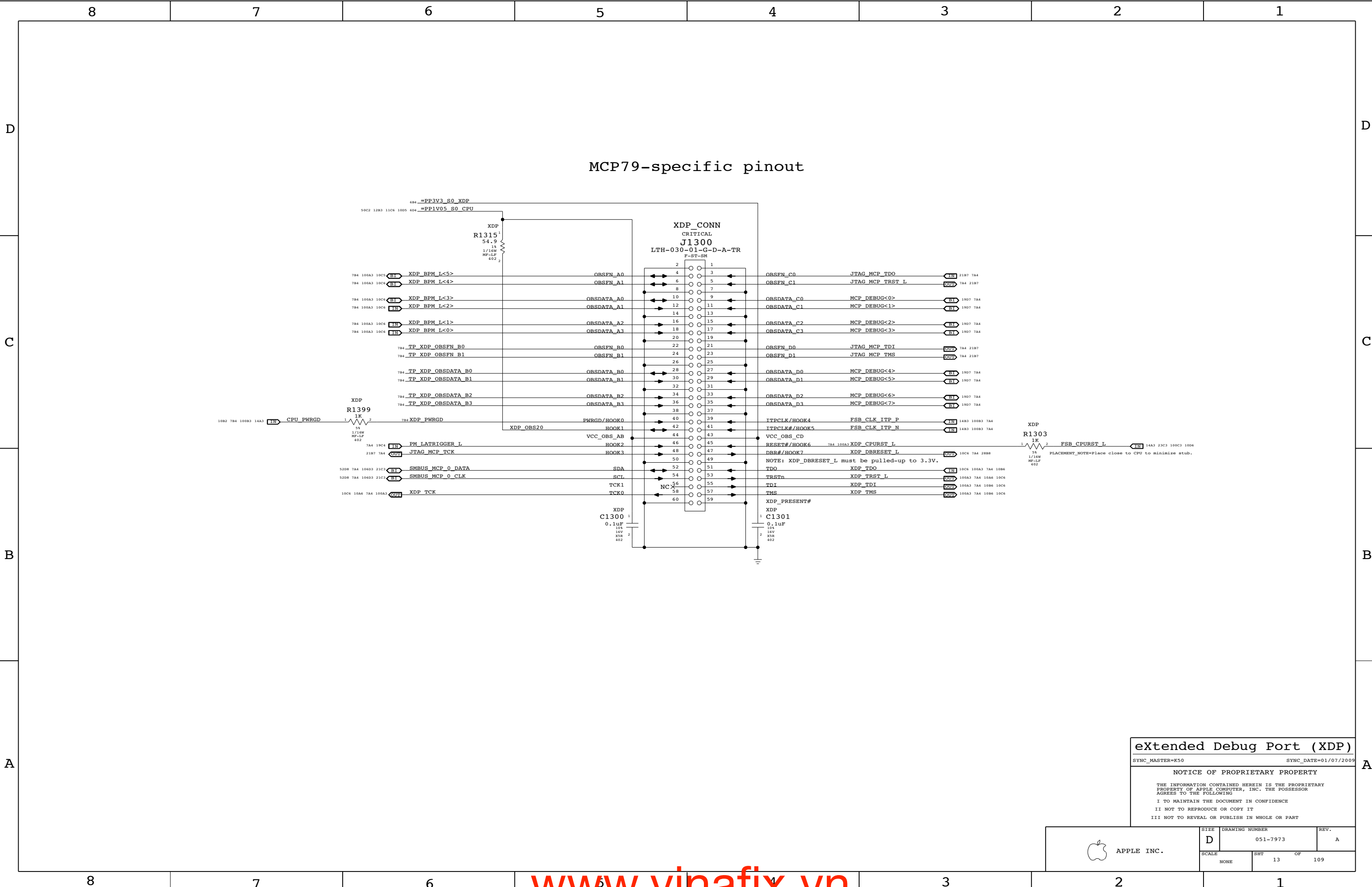
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SCALE		SHT	OF
NONE		11	109





eXtended Debug Port (XDP)

SYNC\_MASTER=R50 SYNC\_DATE=01/07/2009

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APPLE INC.

SIZE

D

SCALE

NONE

DRAWING NUMBER

051-7973

REV.

A

SHT

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109







D

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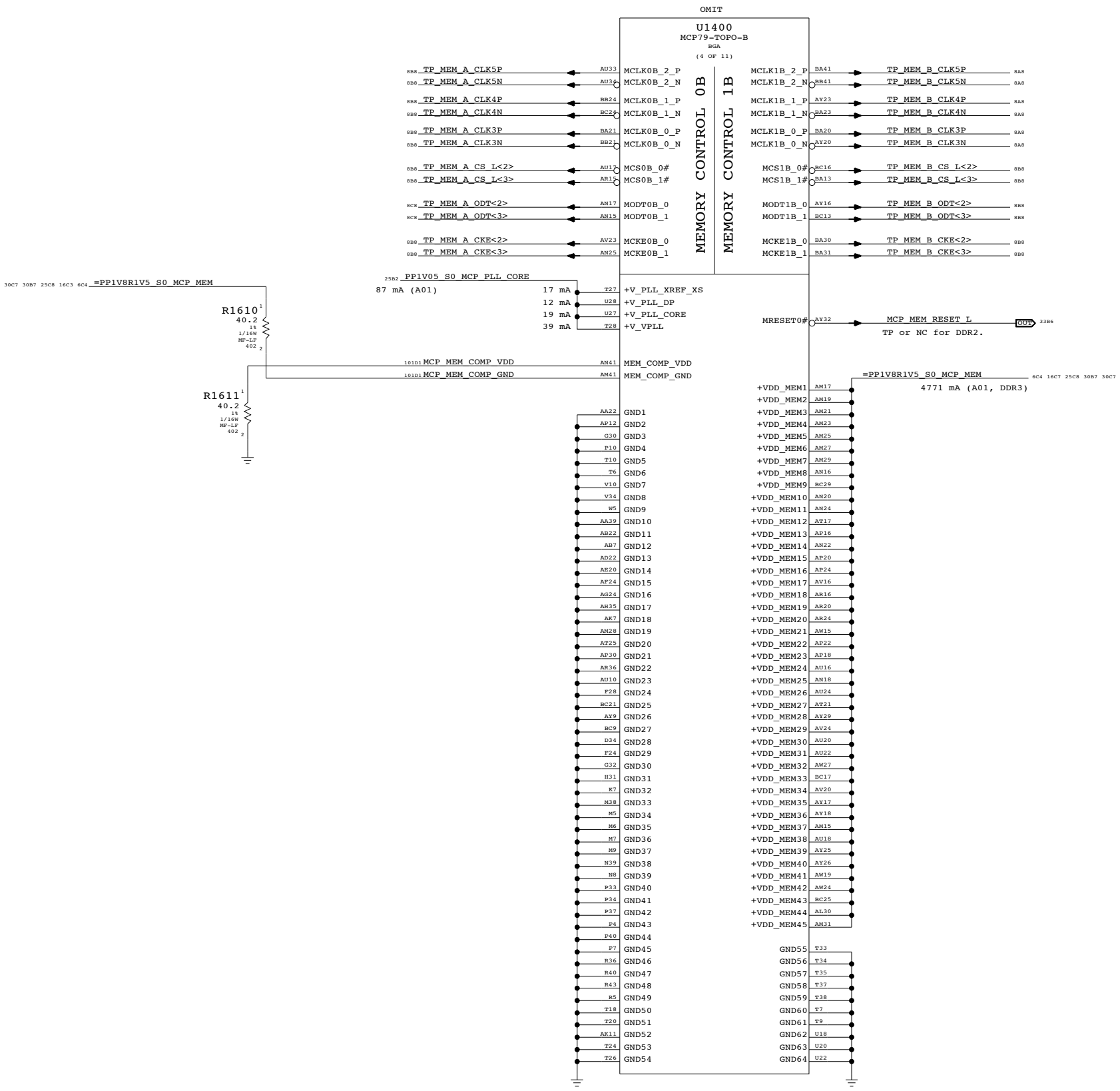
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D

C

B

A



MCP Memory Misc

SYNC\_MASTER=K50

SYNC\_DATE=01/07/2009


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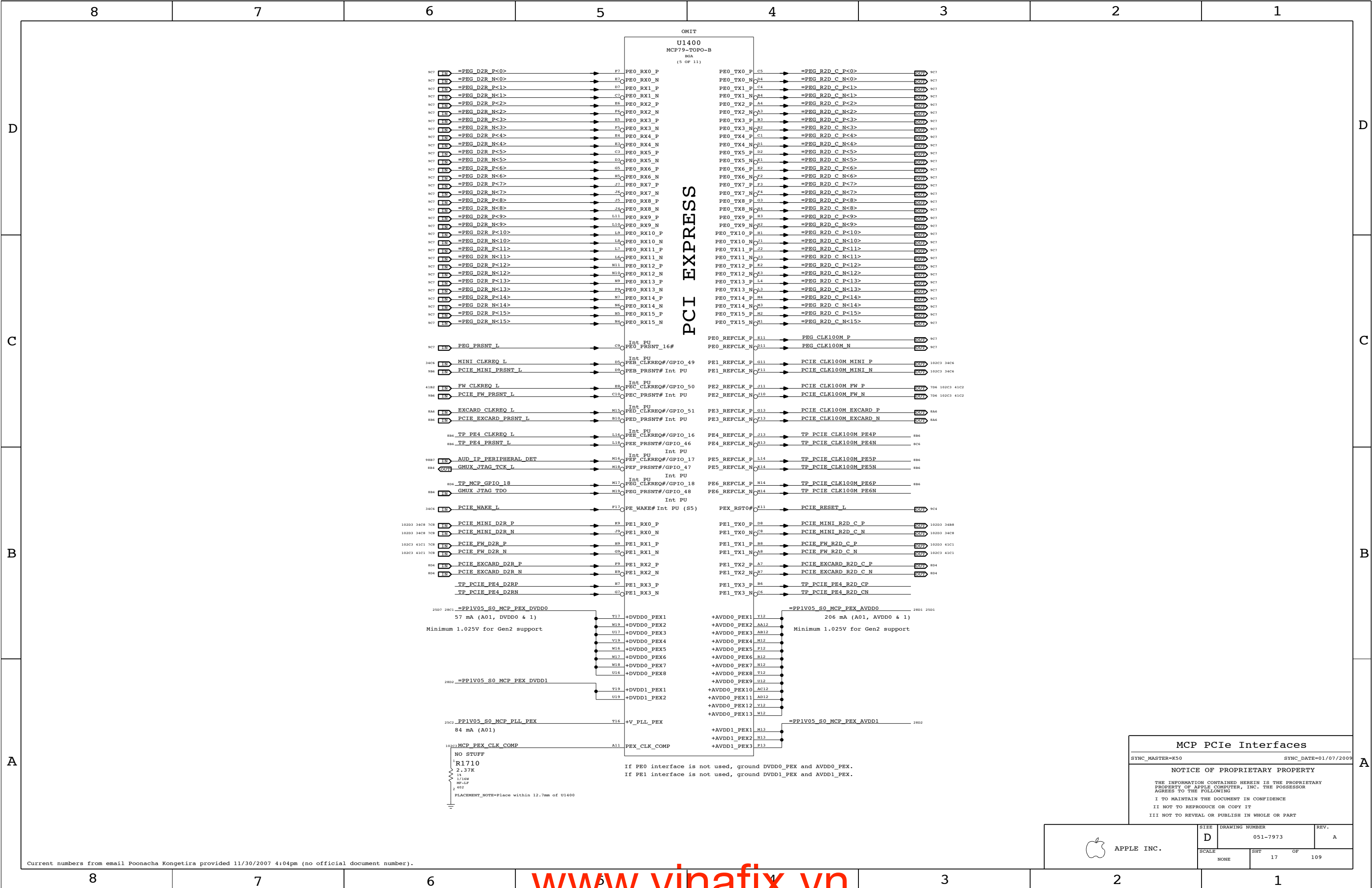
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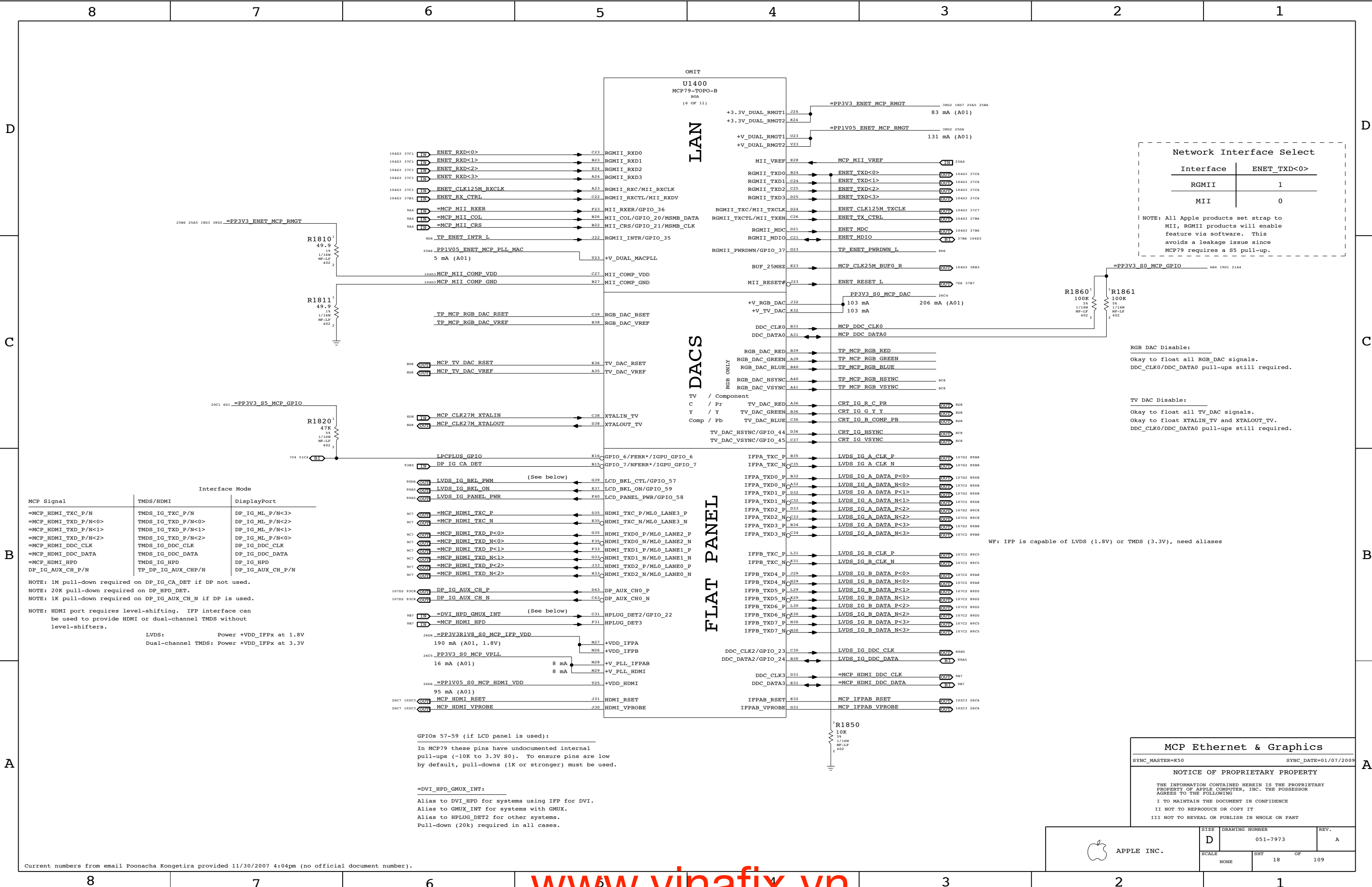
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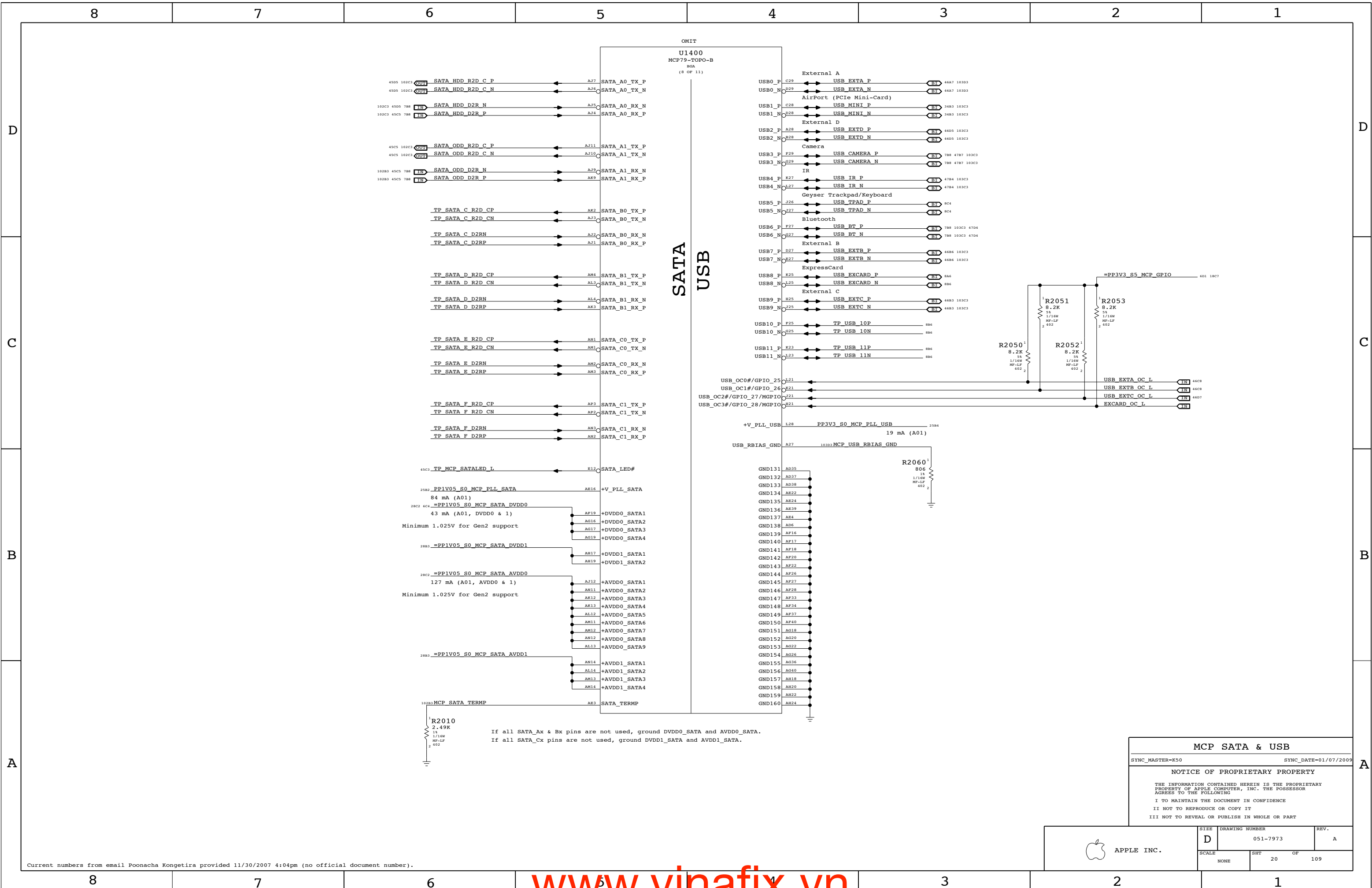
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SCALE		SHT	OF
NONE		16	109











MCP SATA & USB

SYNC\_MASTER=K50

SYNC\_DATE=01/07/2009

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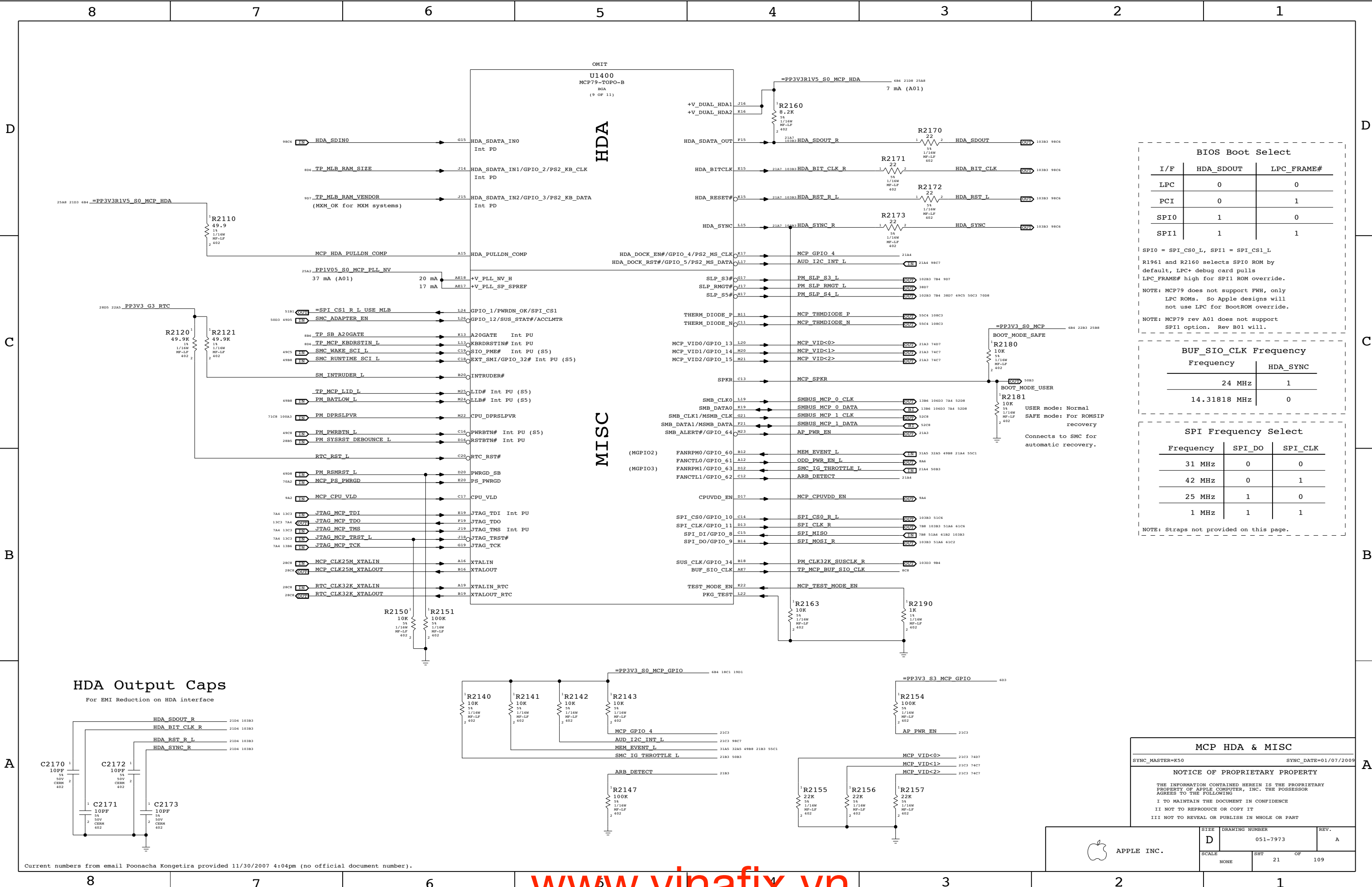
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NONE		20	109



BIOS Boot Select		
I/F	HDA_SDOUT	LPC_FRAME#
LPC	0	0
PCI	0	1
SPI0	1	0
SPI1	1	1

SPI0 = SPI\_CS0\_L, SPI1 = SPI\_CS1\_L

R1961 and R2160 selects SPI0 ROM by default, LPC+ debug card pulls LPC\_FRAME# high for SPI1 ROM override.

NOTE: MCP79 does not support FWH, only LPC ROMs. So Apple designs will not use LPC for BootROM override.

NOTE: MCP79 rev A01 does not support SPI1 option. Rev B01 will.

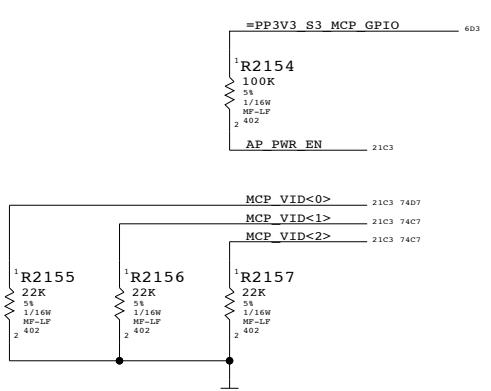
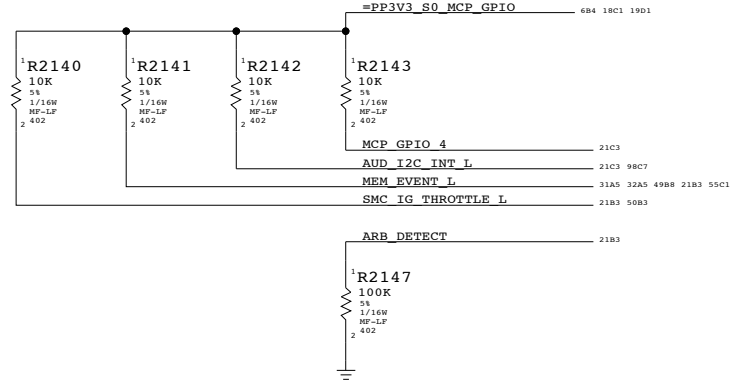
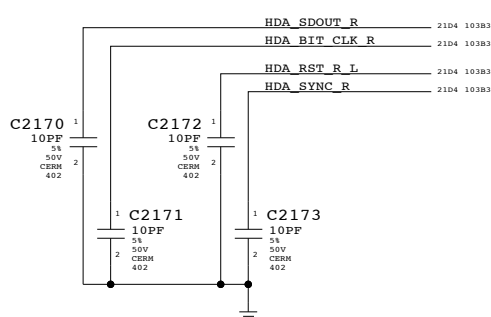
BUF_SIO_CLK Frequency	
Frequency	HDA_SYNC
24 MHz	1
14.31818 MHz	0

SPI Frequency Select		
Frequency	SPI_DO	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

NOTE: Straps not provided on this page.

### HDA Output Caps

For EMI Reduction on HDA interface



MCP HDA & MISC

SYNC\_MASTER=K50      SYNC\_DATE=01/07/2009

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SIZE

D

DRAWING NUMBER

051-7973

REV.

A

SCALE

NONE

SHT

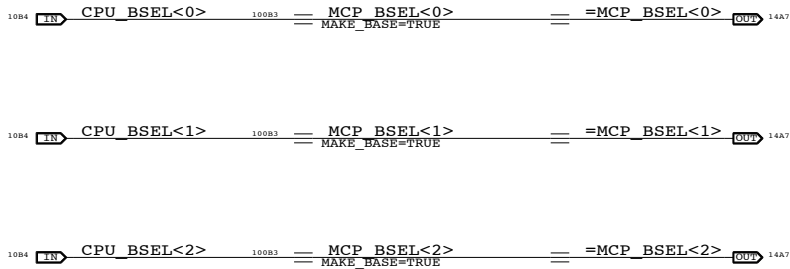
21

OF

109



### CPU FSB Frequency Straps



BSEL<2..0>	FSB MHz
000	266
001	133
010	200
011	(166)
100	333
101	100
110	(400)
111	(RSVD)

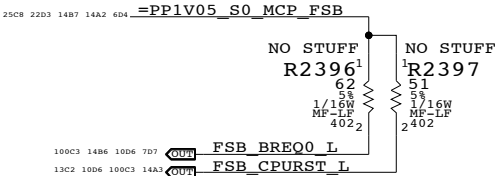
NOTE: ( ) values not supported by MCP79.

Merom/Penryn do not officially support PECI, but it's not clear whether PECI interface is present or not. T12 used pin F6.



### Extra FSB Pull-ups

Exist in MRB but not Intel designs. Here for CYA.  
If found to be necessary, will move to page14.csa



Debug: CPU

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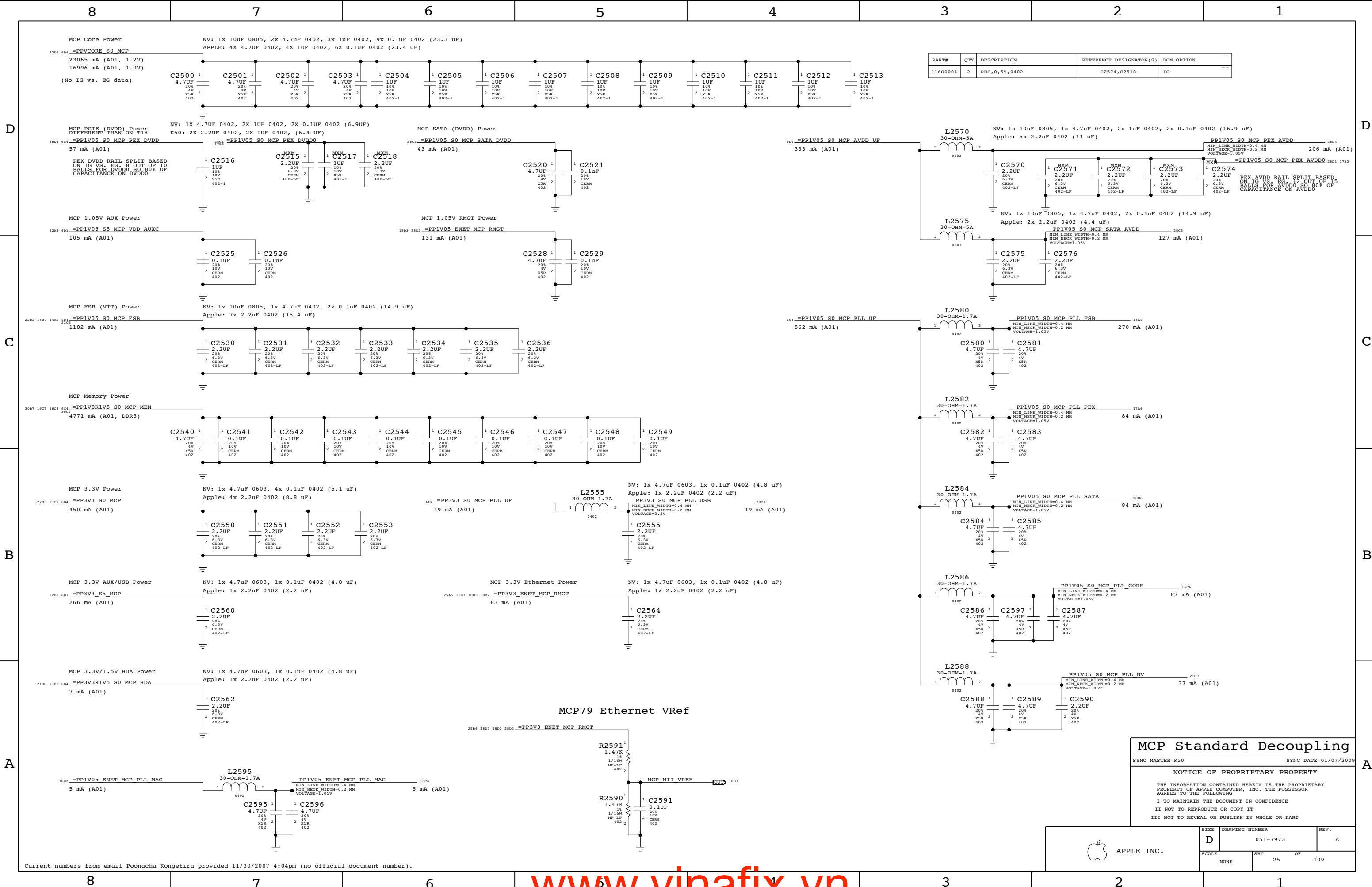
NONE

SHT

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OF

109



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
116S0004	2	RES,0,58,0402	C2574,C2518	IG

### MCP Standard Decoupling

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SIZE	DRAWING NUMBER	REV.
D	051-7973	A
SCALE	SHT	OF
NONE	25	109







## Page Notes

Power aliases required by this page:

- =PP3V3\_S3\_VREFMRGN
- =PP3V3\_S5\_VREFMRGN
- =PPVTT\_S3\_DDR\_BUF

Signal aliases required by this page:

- =I2C\_VREFDACS\_SCL
- =I2C\_VREFDACS\_SDA
- =I2C\_PCA9557D\_SCL
- =I2C\_PCA9557D\_SDA

BOM options provided by this page:  
VREFMRGN

DAC channel  
Min DAC code  
Max DAC code  
Max sink I  
Max source I  
Nominal Vref  
Min Vref  
Max Vref  
Vref Stepping  
(per DAC LSB)

MEM A VREF DQ  
A  
0x00  
0x87  
-3.75 mA  
5 mA  
0.75 V  
0.375 V  
1.250 V  
6.5 mV

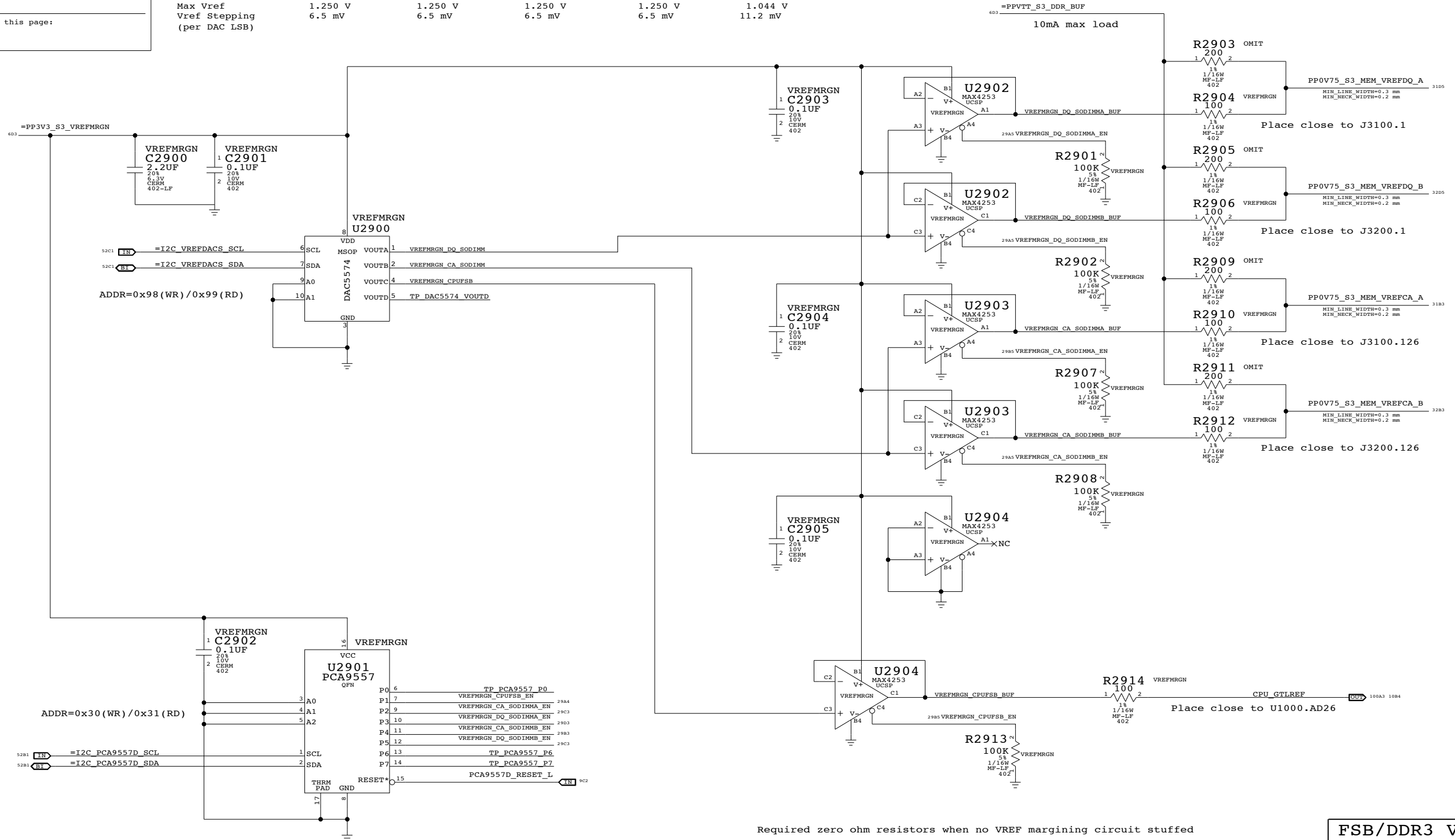
MEM A VREF CA  
B  
0x00  
0x87  
-3.75 mA  
5 mA  
0.75 V  
0.375 V  
1.250 V  
6.5 mV

MEM B VREF DQ  
A  
0x00  
0x87  
-3.75 mA  
5 mA  
0.75 V  
0.375 V  
1.250 V  
6.5 mV

MEM B VREF CA  
B  
0x00  
0x87  
-3.75 mA  
5 mA  
0.75 V  
0.375 V  
1.250 V  
6.5 mV

CPU FSB VREF  
C  
0x00  
0x55  
-0.91 mA  
0.52 mA  
0.70 V  
0.091 V  
1.044 V  
11.2 mV

SO-DIMM A and SO-DIMM B Vref settings should be margined separately  
(i.e. not simultaneously) due to current limitation of TPS51116 regulator.



Required zero ohm resistors when no VREF margining circuit stuffed

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
11480149	1	RES,402,1/16W,200 OHM,1%	R2903		VREFMRGN
11680004	1	RES,402,1/16W,0 OHM,5%	R2903		PRODUCTION
11480149	1	RES,402,1/16W,200 OHM,1%	R2905		VREFMRGN
11680004	1	RES,402,1/16W,0 OHM,5%	R2905		PRODUCTION
11480149	1	RES,402,1/16W,200 OHM,1%	R2909		VREFMRGN
11680004	1	RES,402,1/16W,0 OHM,5%	R2909		PRODUCTION
11480149	1	RES,402,1/16W,200 OHM,1%	R2911		VREFMRGN
11680004	1	RES,402,1/16W,0 OHM,5%	R2911		PRODUCTION

## FSB/DDR3 Vref Margining

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SYNC\_DATE=01/07/2009

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SIZE

D

DRAWING NUMBER

051-7973

REV.

A

SCALE

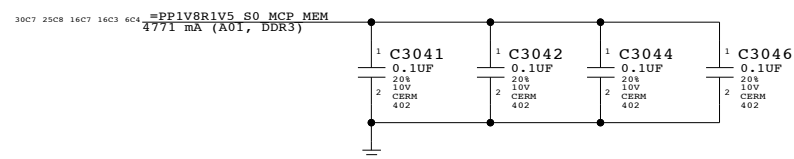
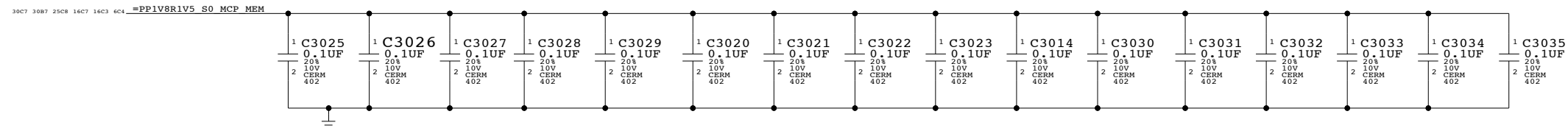
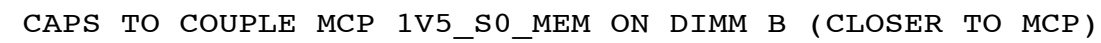
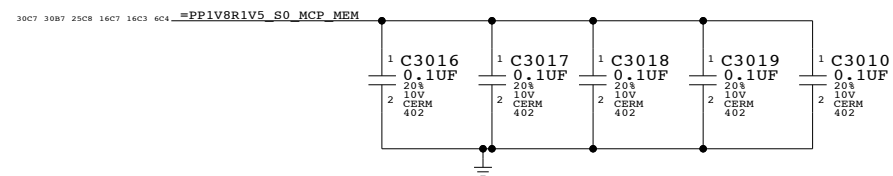
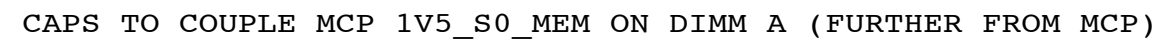
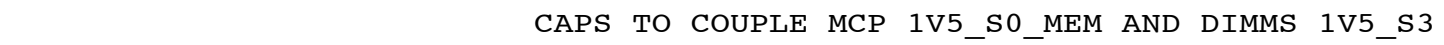
NONE

SHT


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OF

109



MEMORY COUPLING CAPS	
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	D	051-7973	A
	SCALE	SHT	OF
	NONE	30	109





## Page Notes

Power aliases required by this page:

```
- =PP1V5_S0_MEM_B
- =PP1V5_S3_MEM_B
- =PP0V75_S0_MEM_VTT_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)
```

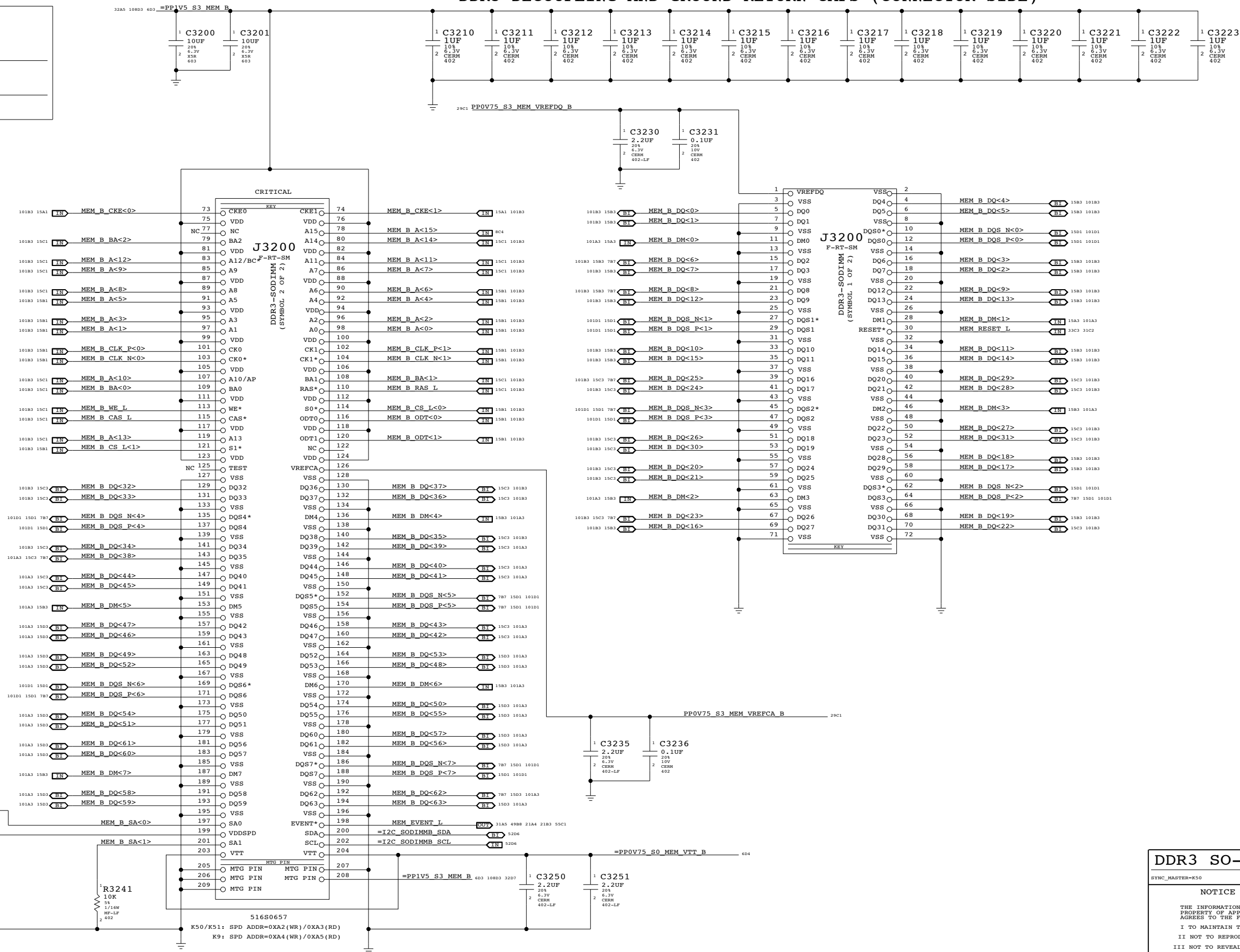
Signal aliases required by this page:

```
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA
```

BOM options provided by this pager:

(NONE)

## DDR3 DECOUPLING AND GROUND RETURN CAPS (CONNECTOR SIDE)



## DDR3 SO-DIMM CONNECTOR B

SYNC MASTER=K50

SYNC DATE=01/07/2009

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ST2

51

1

SCA

DRAWING NUMBER
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253

1

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143	144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159	160	161	162	163	164	165	166	167	168	169	170	171	172	173	174	175	176	177	178	179	180	181	182	183	184	185	186	187	188	189	190	191	192	193	194	195	196	197	198	199	200	201	202	203	204	205	206	207	208	209	210	211	212	213	214	215	216	217	218	219	220	221	222	223	224	225	226	227	228	229	230	231	232	233	234	235	236	237	238	239	240	241	242	243	244	245	246	247	248	249	250	251	252	253	254	255	256	257	258	259	260	261	262	263	264	265	266	267	268	269	270	271	272	273	274	275	276	277	278	279	280	281	282	283	284	285	286	287	288	289	290	291	292	293	294	295	296	297	298	299	300	301	302	303	304	305	306	307	308	309	310	311	312	313	314	315	316	317	318	319	320	321	322	323	324	325	326	327	328	329	330	331	332	333	334	335	336	337	338	339	340	341	342	343	344	345	346	347	348	349	350	351	352	353	354	355	356	357	358	359	360	361	362	363	364	365	366	367	368	369	370	371	372	373	374	375	376	377	378	379	380	381	382	383	384	385	386	387	388	389	390	391	392	393	394	395	396	397	398	399	400	401	402	403	404	405	406	407	408	409	410	411	412	413	414	415	416	417	418	419	420	421	422	423	424	425	426	427	428	429	430	431	432	433	434	435	436	437	438	439	440	441	442	443	444	445	446	447	448	449	450	451	452	453	454	455	456	457	458	459	460	461	462	463	464	465	466
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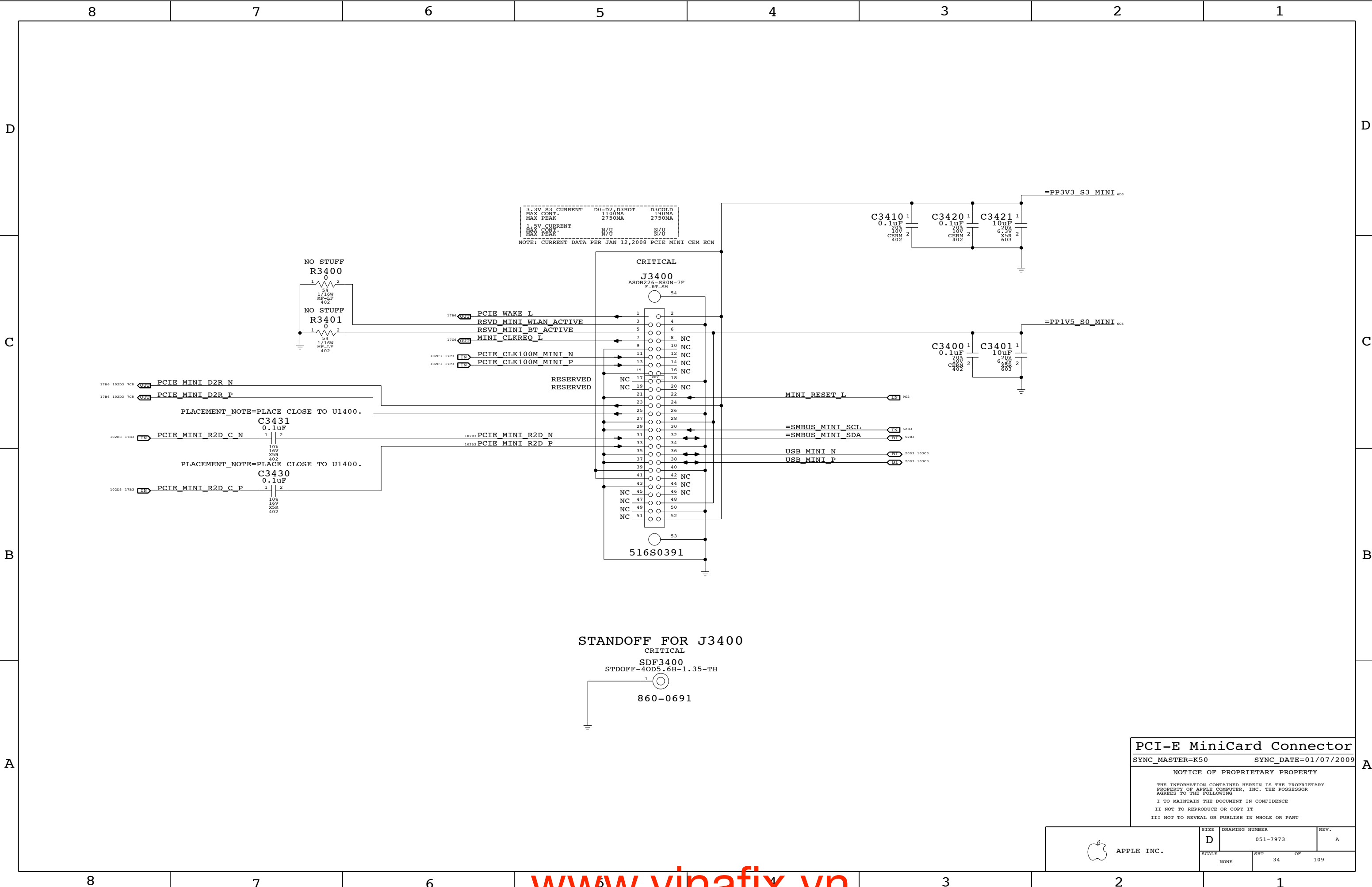
NONE

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REV

TABLE 1





PCI-E MiniCard Connector

SYNC\_MASTER=K50 SYNC\_DATE=01/07/2009

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SIZE D	DRAWING NUMBER 051-7973	REV. A
SCALE NONE	SHT 34	OF 109



SIGNAL MODEL=EMPTY  
R3880

1 2

5W  
1/16W  
NF-LF  
40.2

ENET\_EN 38A8 38B8

PM\_SLP\_RMGT\_L

PM\_SLP\_S4\_L

SIGNAL MODEL=EMPTY  
NO STUFF  
R3881

1 2

5W  
1/16W  
NF-LF  
40.2

```

38C5 PP1V05_RMGTT                == PP1V05_ENET MCP_RMGTT                1803 2506
                                   == PP1V05_ENET MCP_PLL_MAC            25A8
                                   == PP1V05_ENET_PHY                    37D2

38B0 PP3V3_RMGTT                == PP3V3_ENET MCP_RMGTT                1803 18D7 25A5 25B6
                                   == PP3V3_ENET_PHY                    37D7

                                   == RTL8211_ENSWREG                    37C6
MAKE_BASE=TRUE
NOTE: NOT USING THE BUILT-IN 1.05V REGULATOR OF THE PHY

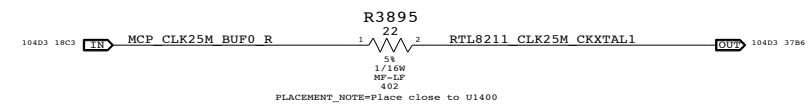
NC RTL8211_REGOUT                == RTL8211_REGOUT                    37C2
MAKE_BASE=TRUE
NO_TEST=TRUE

NC PP3V3_ENET_PHY_VDDREG        == PP3V3_ENET_PHY_VDDREG            37C2
MAKE_BASE=TRUE
NO_TEST=TRUE

```

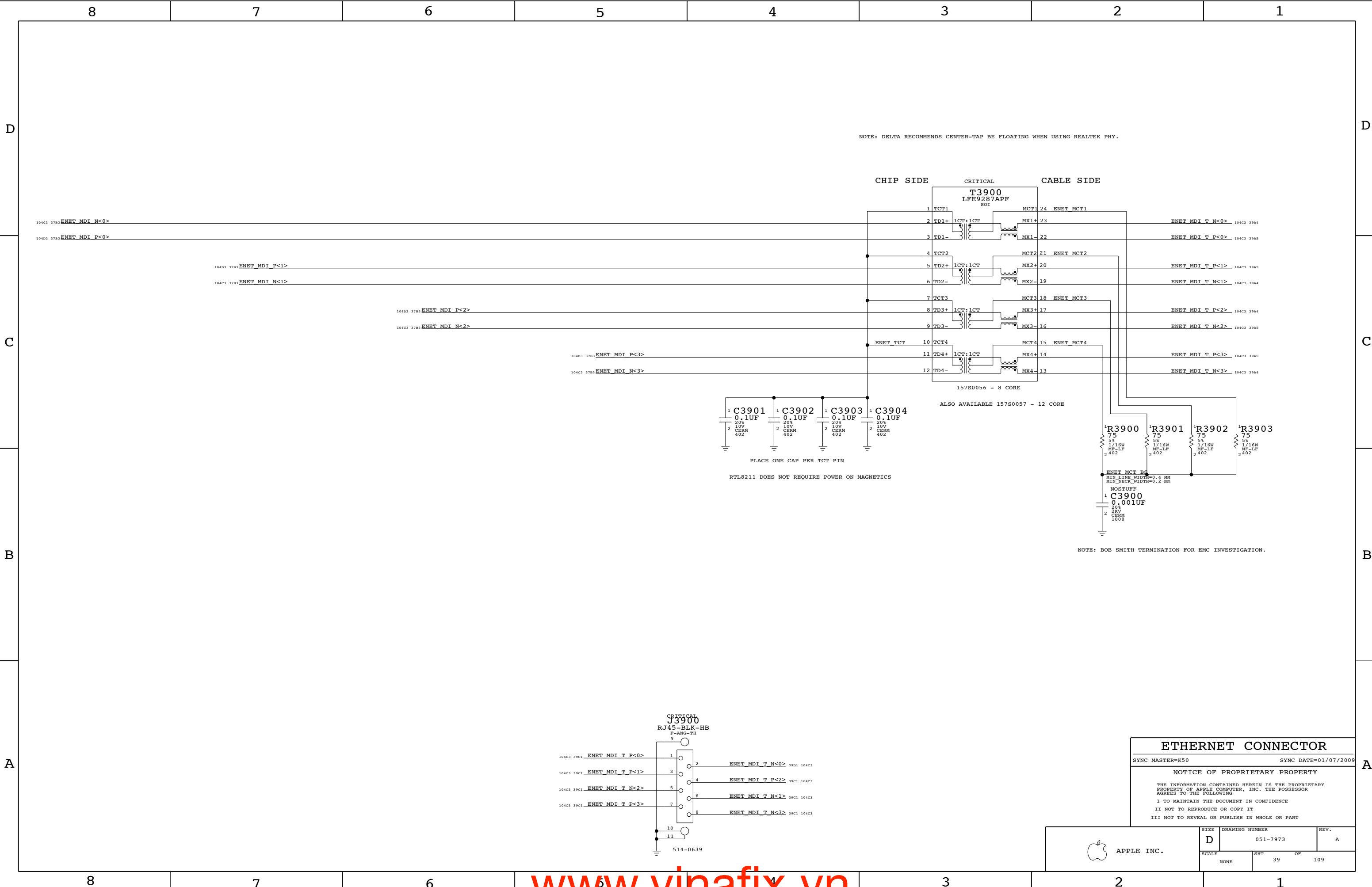
[illegible][illegible]

NOTE: MCP79 can provide 25MHz clock, but clock runs whenever RMGT rails are powered. Designs must ensure PHY is powered whenever RMGT rails are, or use separate crystal.



SYNC_MASTER=K50	SYNC_DATE=01/07/2009
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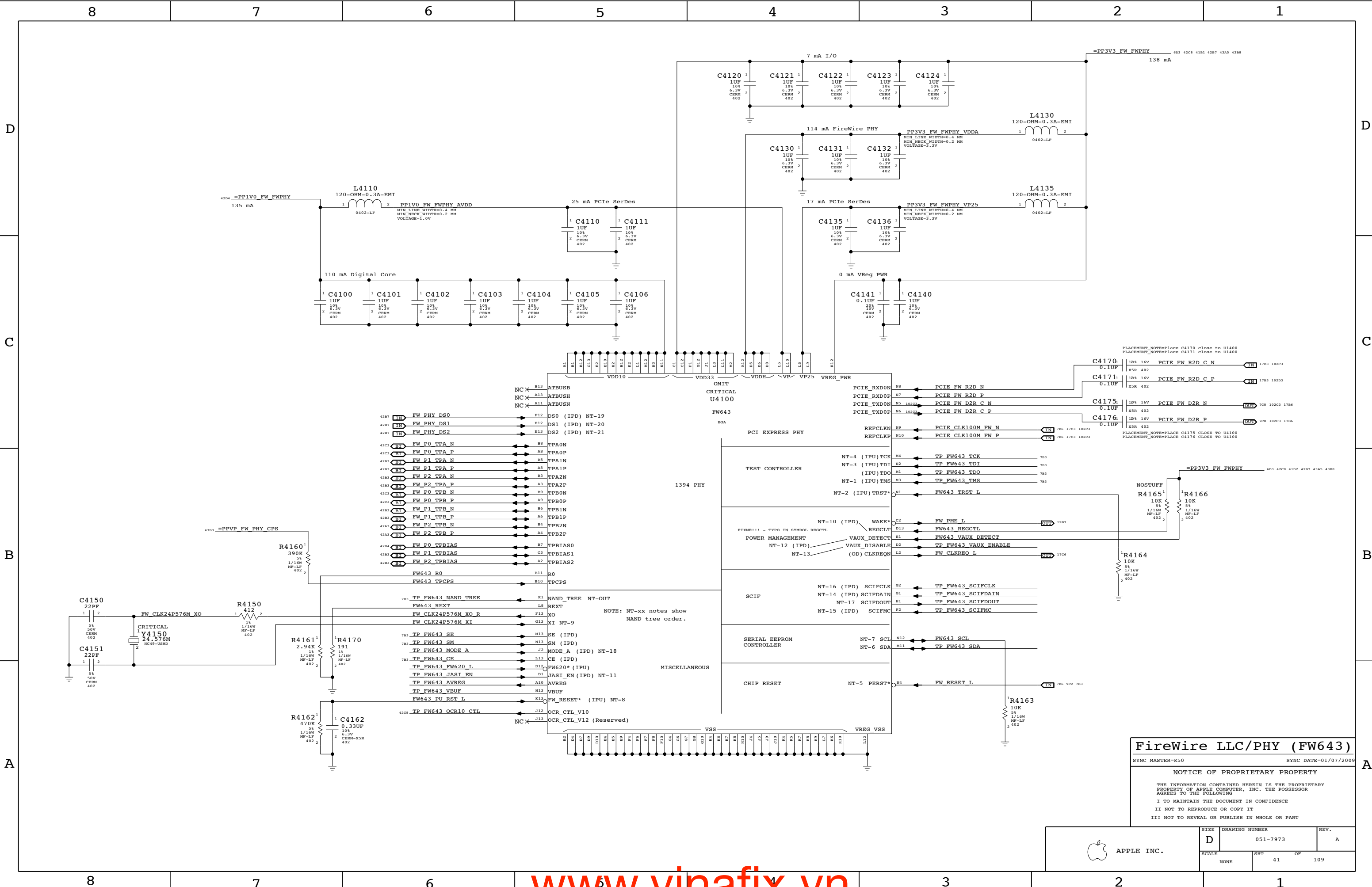
SIZE D	DRAWING NUMBER 051-7973	REV. A
SCALE NONE	SHT 38	OF 109



ETHERNET CONNECTOR
SYNC\_MASTER=K50 SYNC\_DATE=01/07/2009
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Table with 3 columns: SIZE, DRAWING NUMBER, REV. and 2 columns: SCALE, SHT OF 109. Contains Apple logo and text: APPLE INC., D, 051-7973, A, NONE, 39 OF 109.





# FireWire LLC/PHY (FW643)

SYNC\_MASTER=K50 SYNC\_DATE=01/07/2009

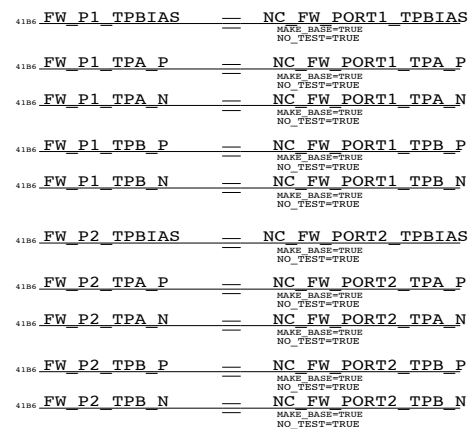
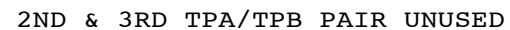
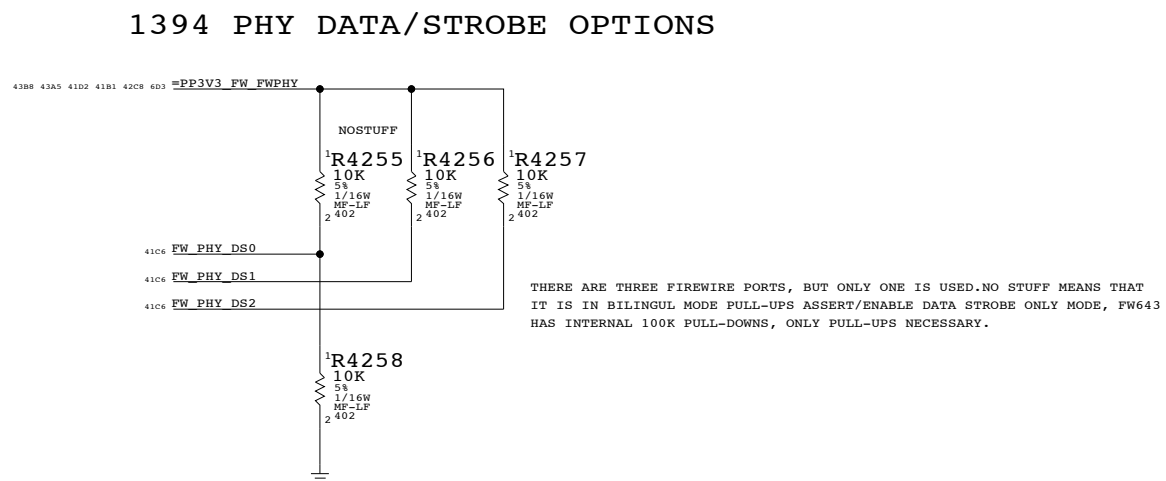
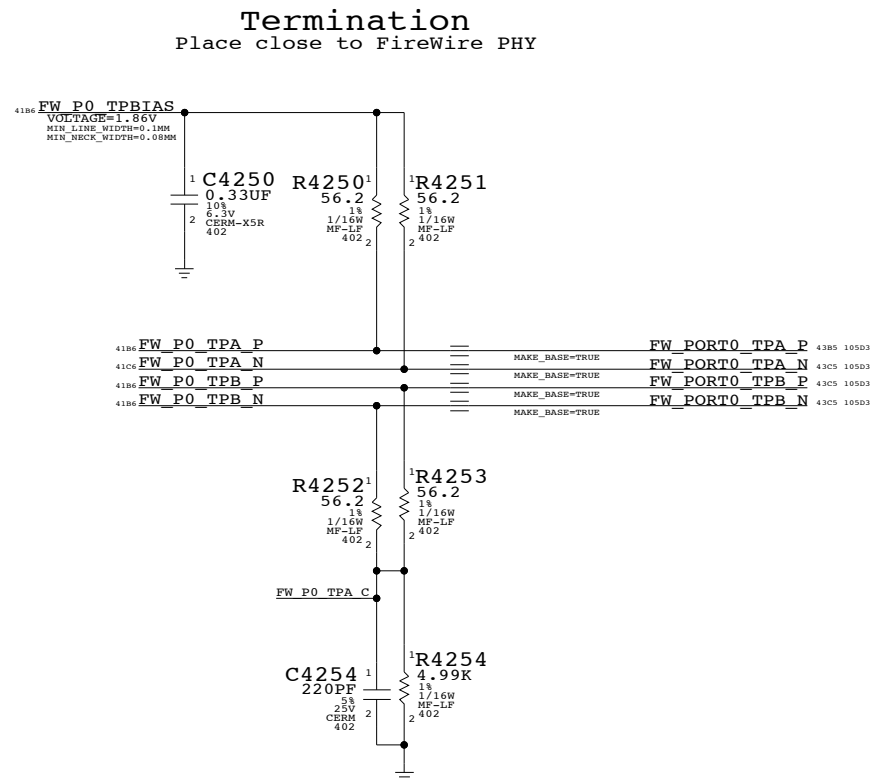
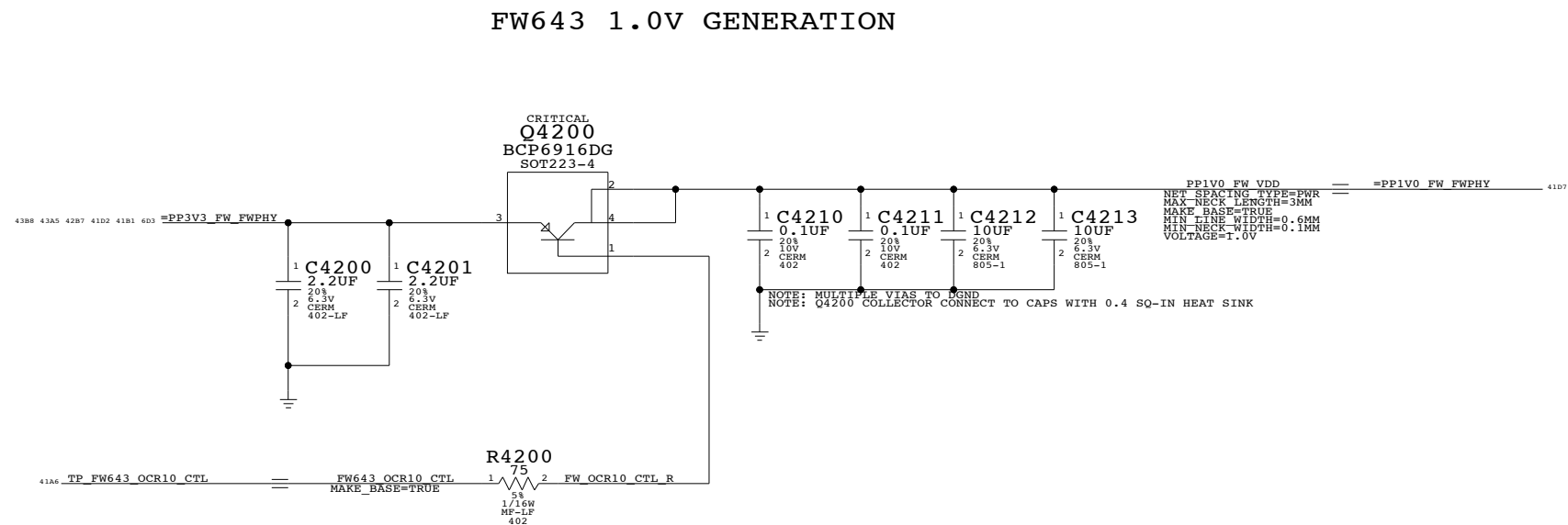
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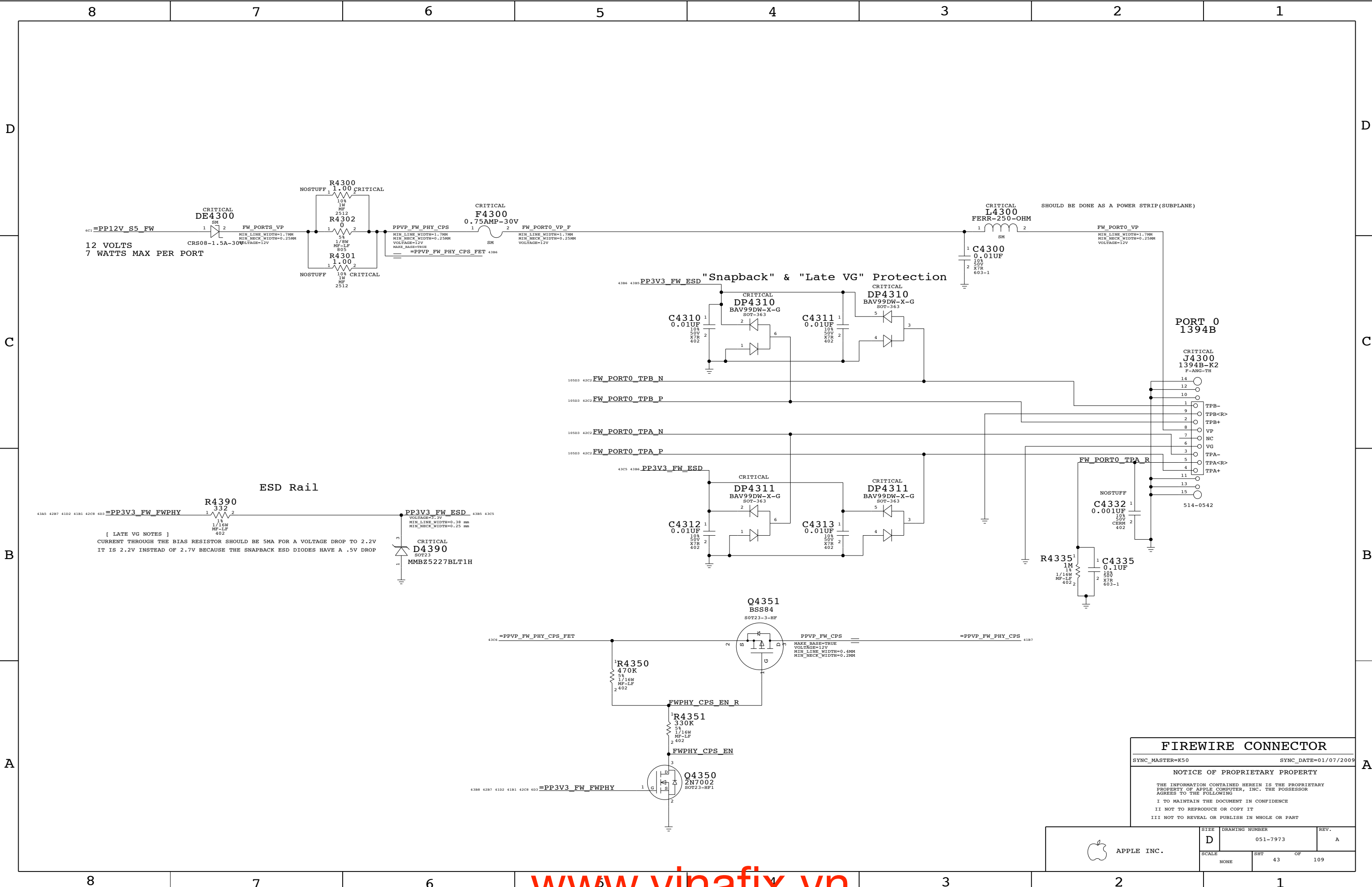
SIZE	DRAWING NUMBER	REV.
D	051-7973	A
SCALE	SHT	OF
NONE	41	109



NOTE: AGERE'S RECOMMENDATION FOR UNUSED PORTS

FW: 1394B MISC	
SYNC_MASTER=K50	SYNC_DATE=01/07/2009
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 APPLE INC.	SIZE <b>D</b>	DRAWING NUMBER 051-7973	REV. A
	SCALE NONE	SHT OF 42 109	



D

C

B

A

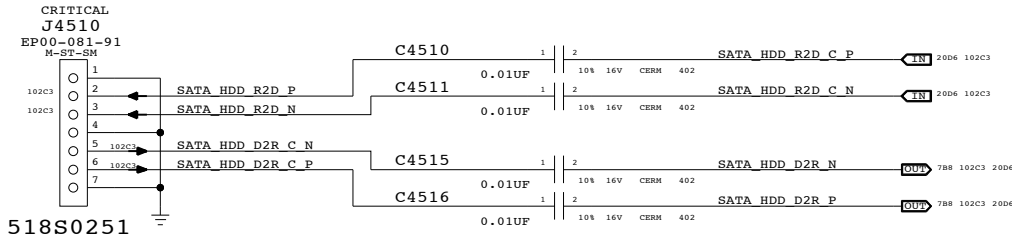
D

C

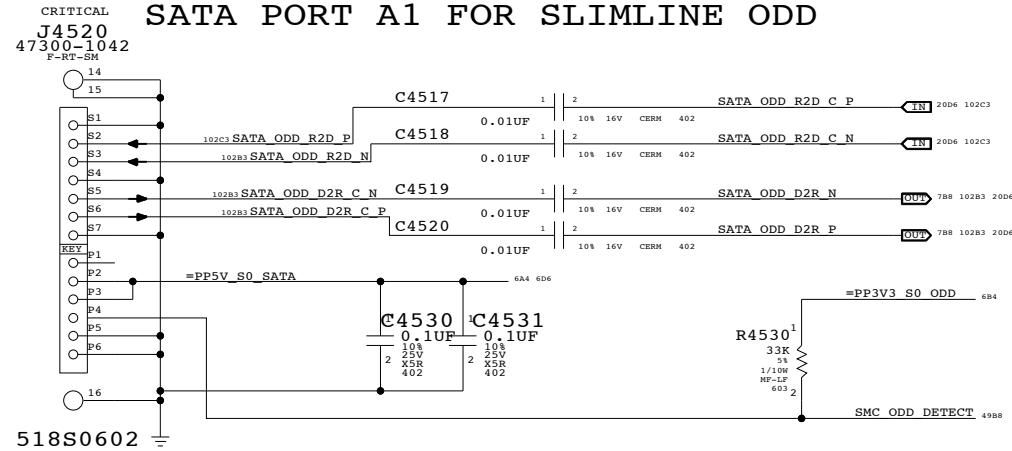
B

A

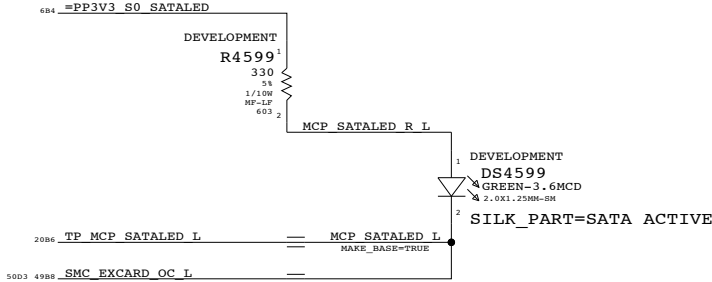
SATA PORT A0 FOR HDD



SATA PORT A1 FOR SLIMLINE ODD



SATA Activity LED



SATA Connectors

SYNC\_MASTER=K50 SYNC\_DATE=01/07/2009

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SIZE  
D

DRAWING NUMBER  
051-7973

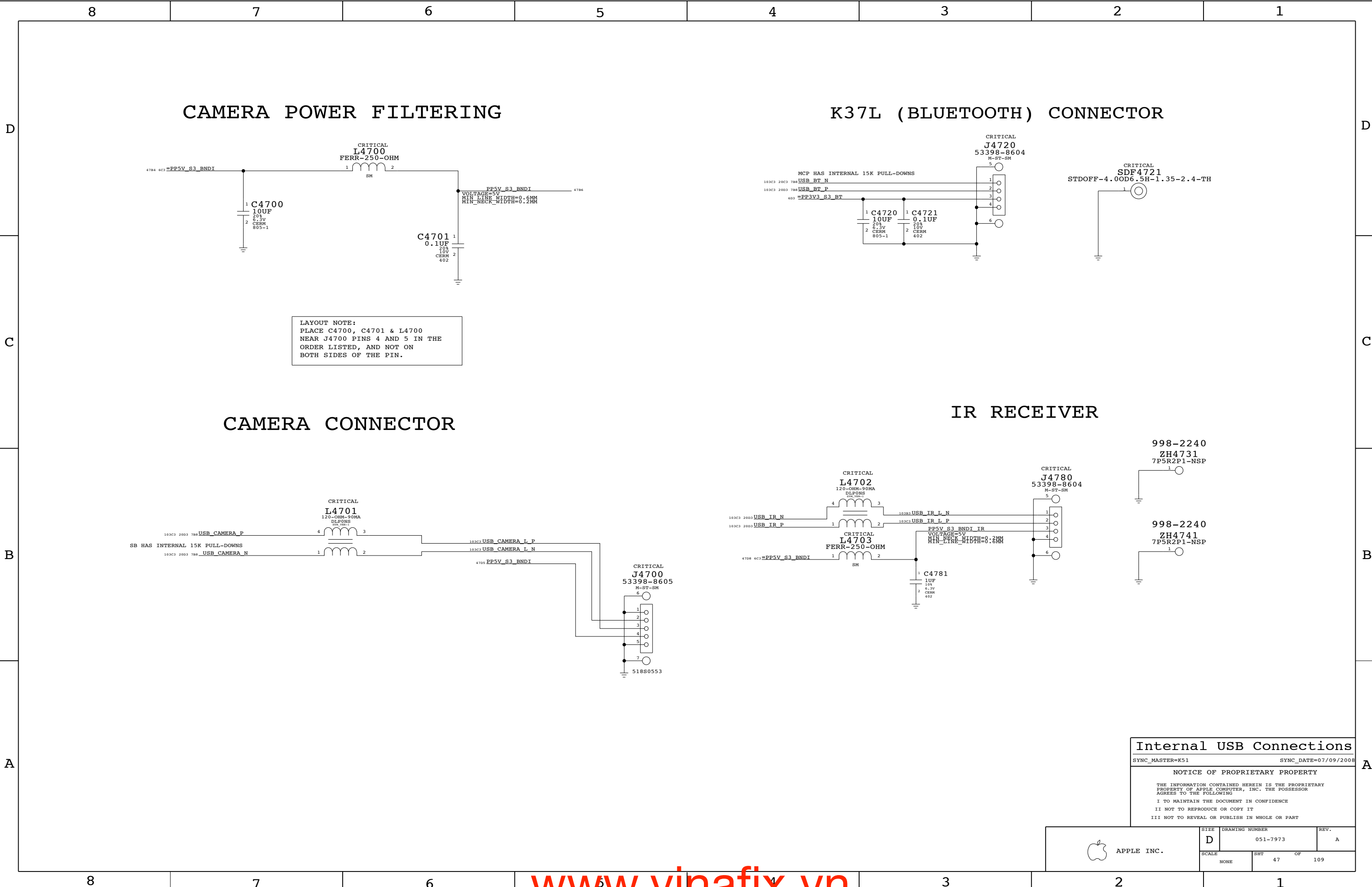
REV.  
A

SCALE  
NONE

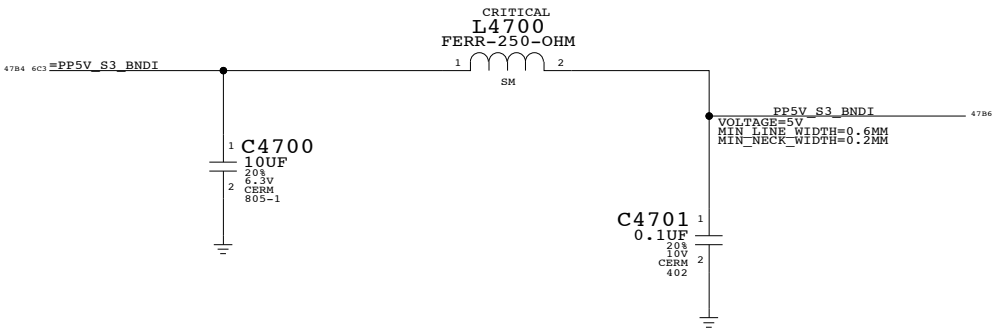
SHT  
45

OF  
109



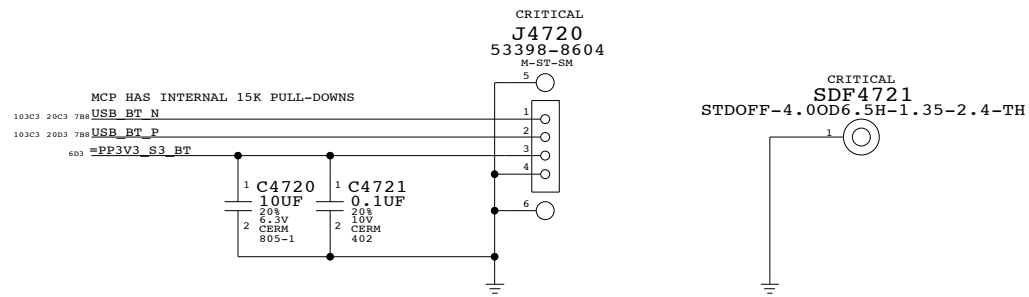


CAMERA POWER FILTERING

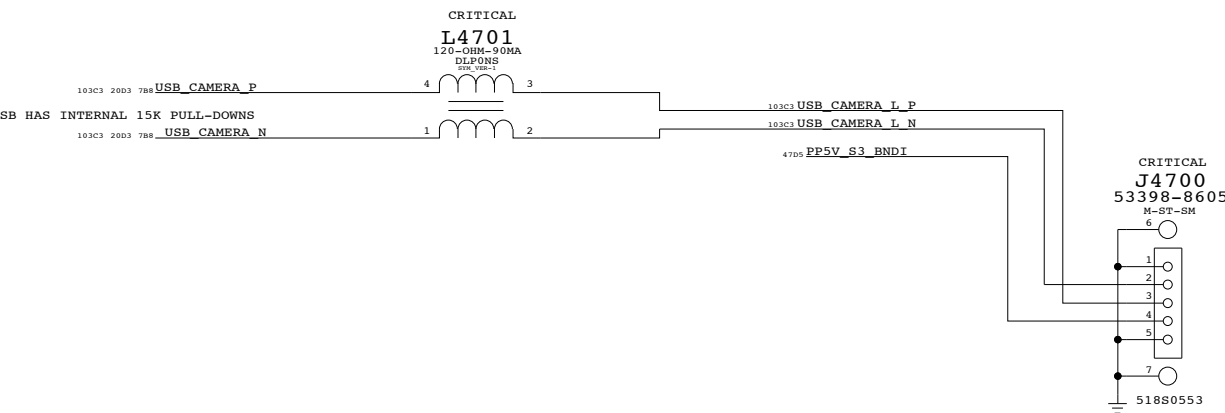


LAYOUT NOTE:  
PLACE C4700, C4701 & L4700  
NEAR J4700 PINS 4 AND 5 IN THE  
ORDER LISTED, AND NOT ON  
BOTH SIDES OF THE PIN.

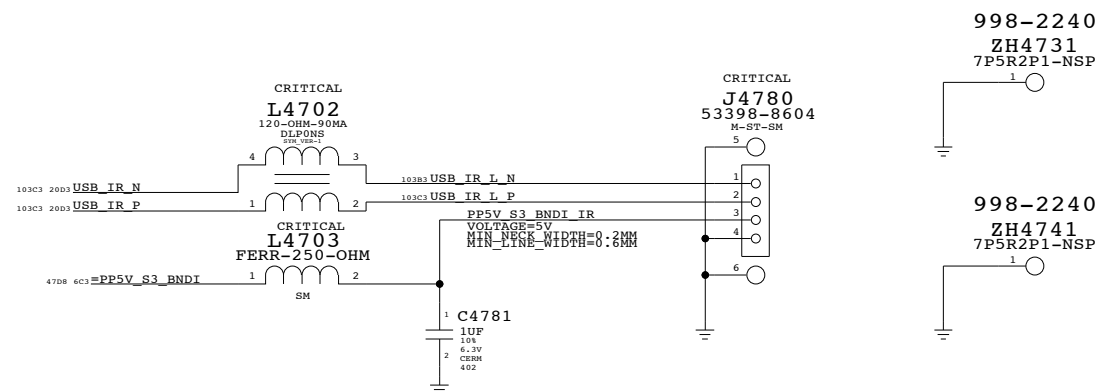
K37L (BLUETOOTH) CONNECTOR



CAMERA CONNECTOR



IR RECEIVER



Internal USB Connections

SYNC\_MASTER=K51 SYNC\_DATE=07/09/2008

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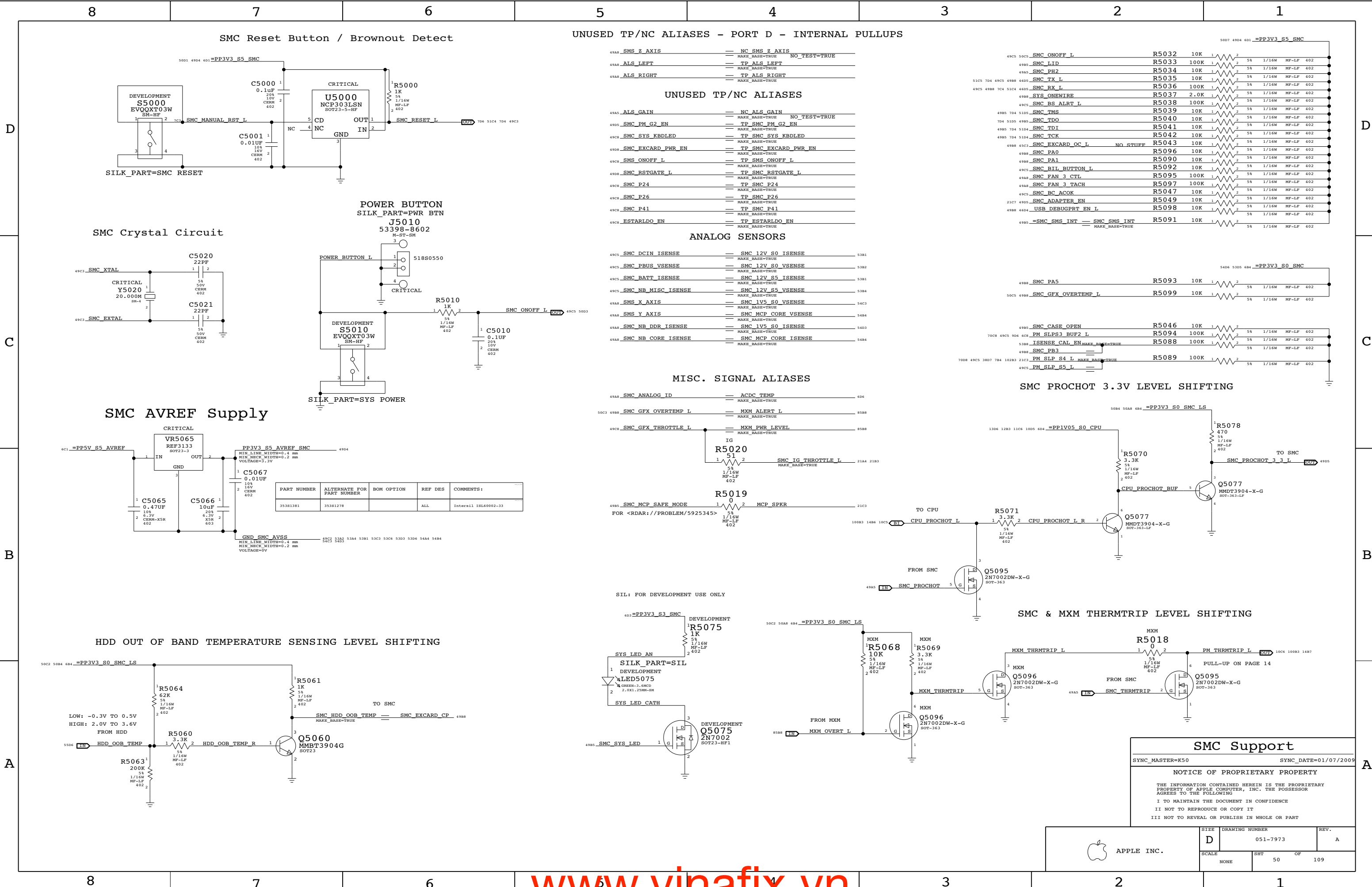


APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7973	A
SCALE	SHT	OF
NONE	47	109







D

C

B

A

D

C

B

A

8	7	6	5	4	3	2	1
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## C



## D

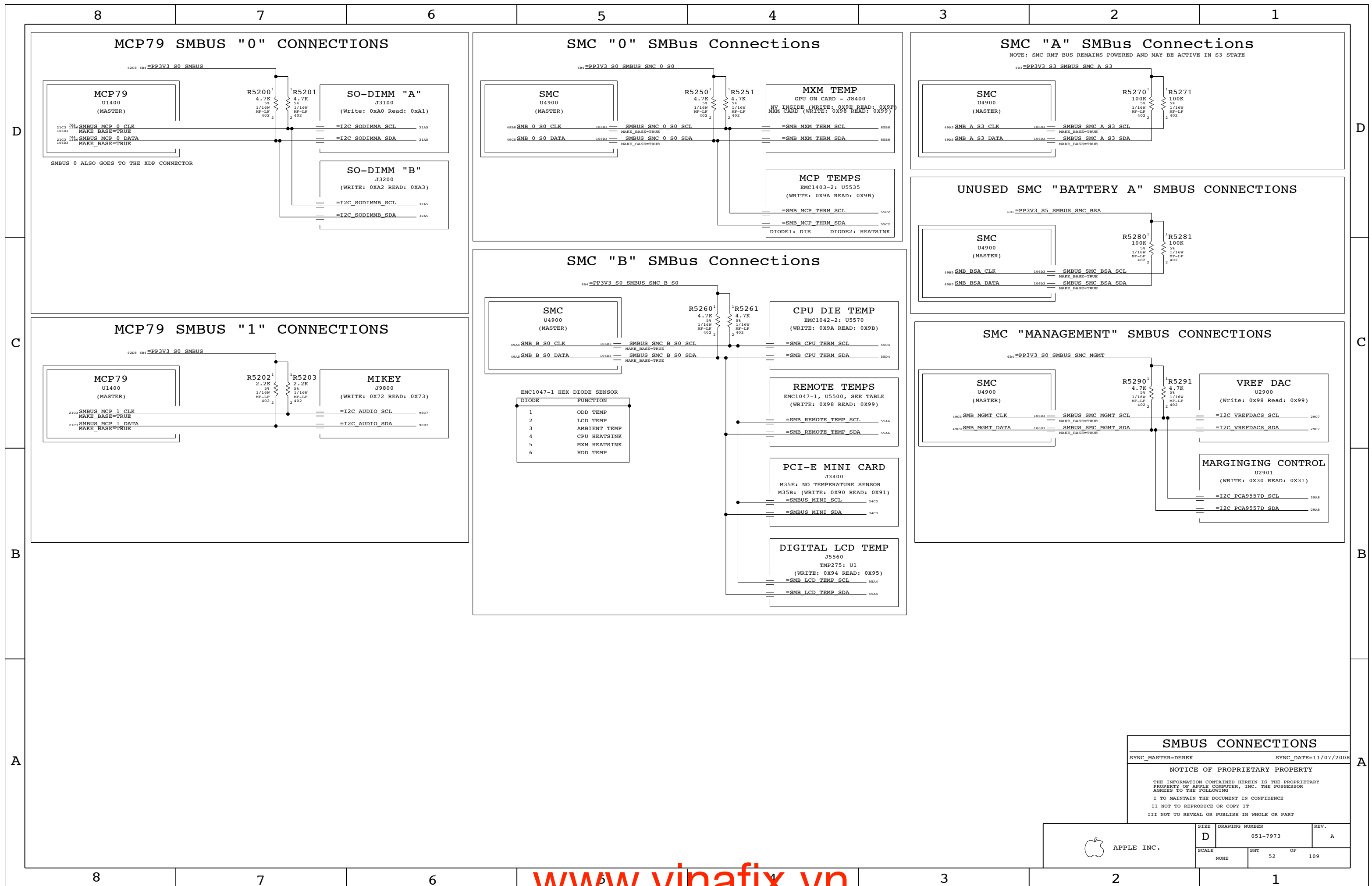
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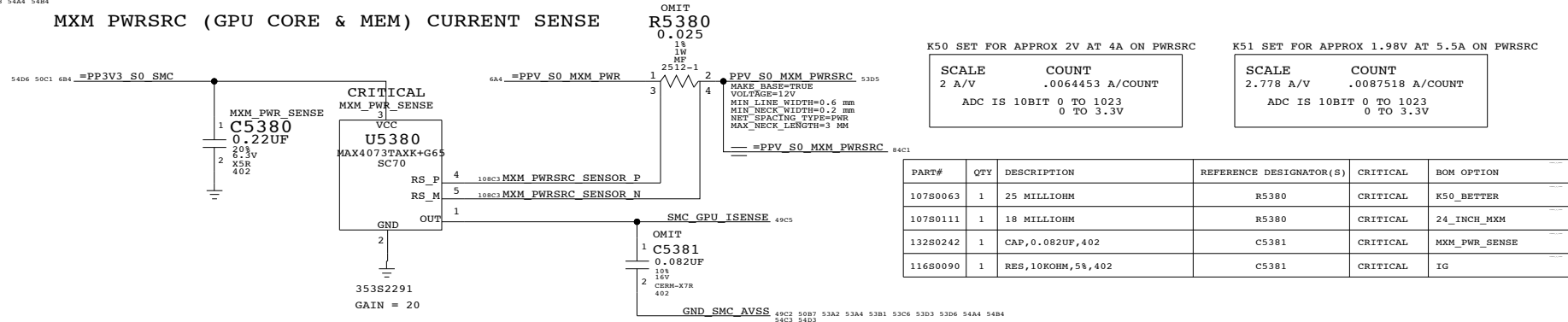
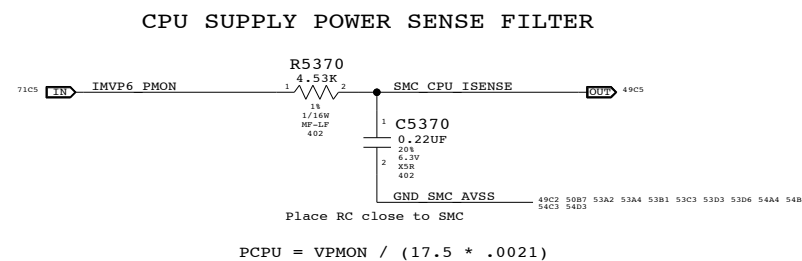
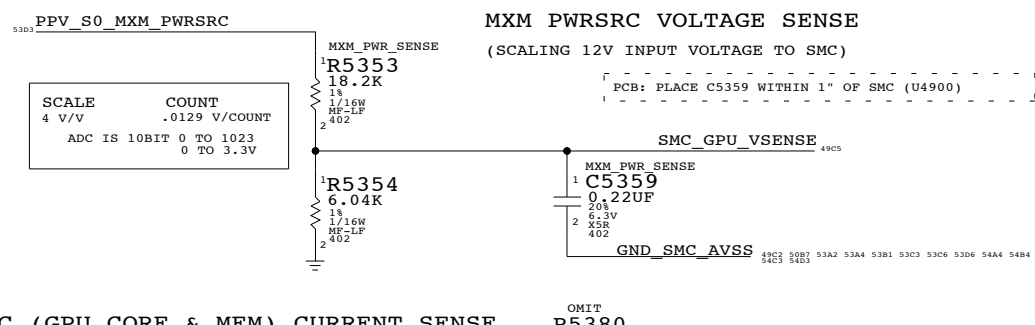
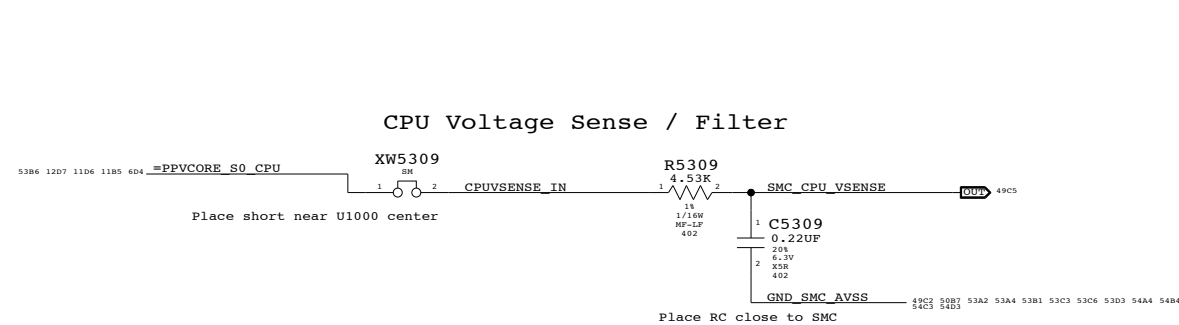


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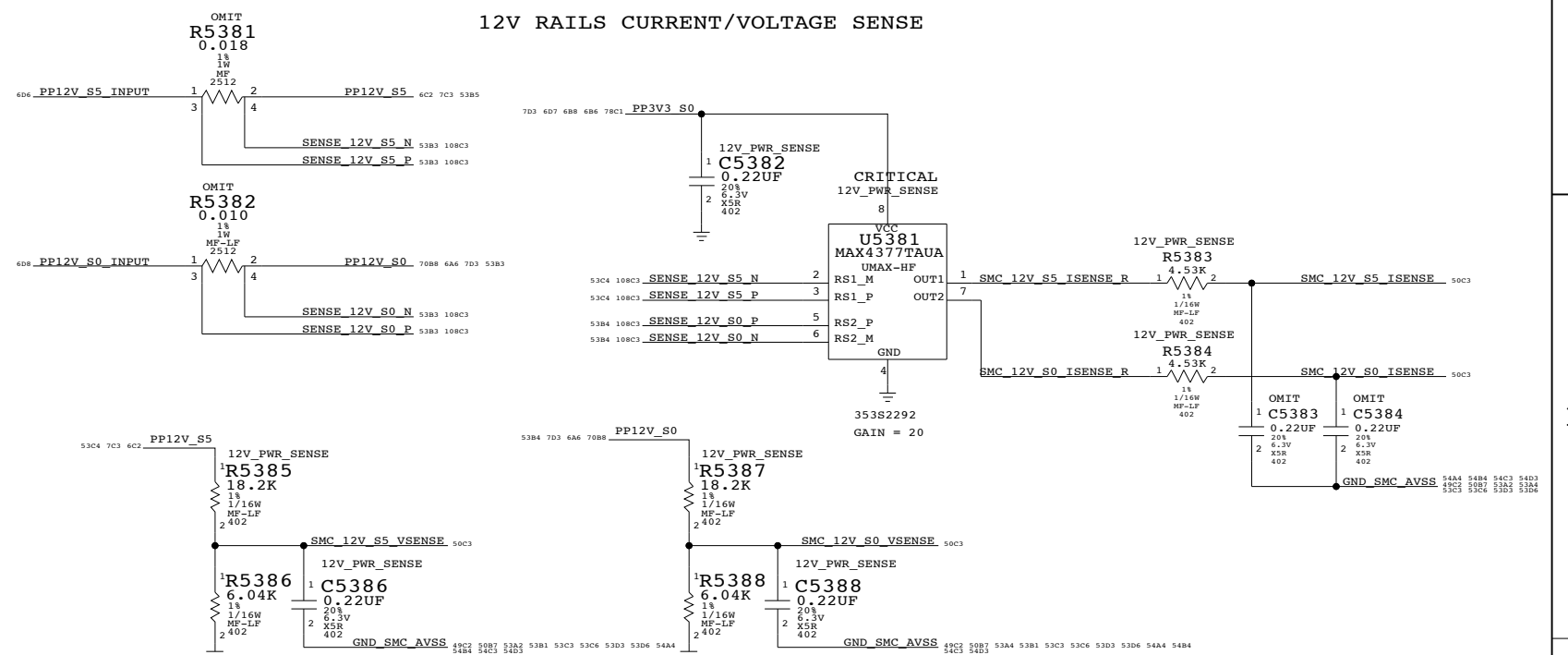
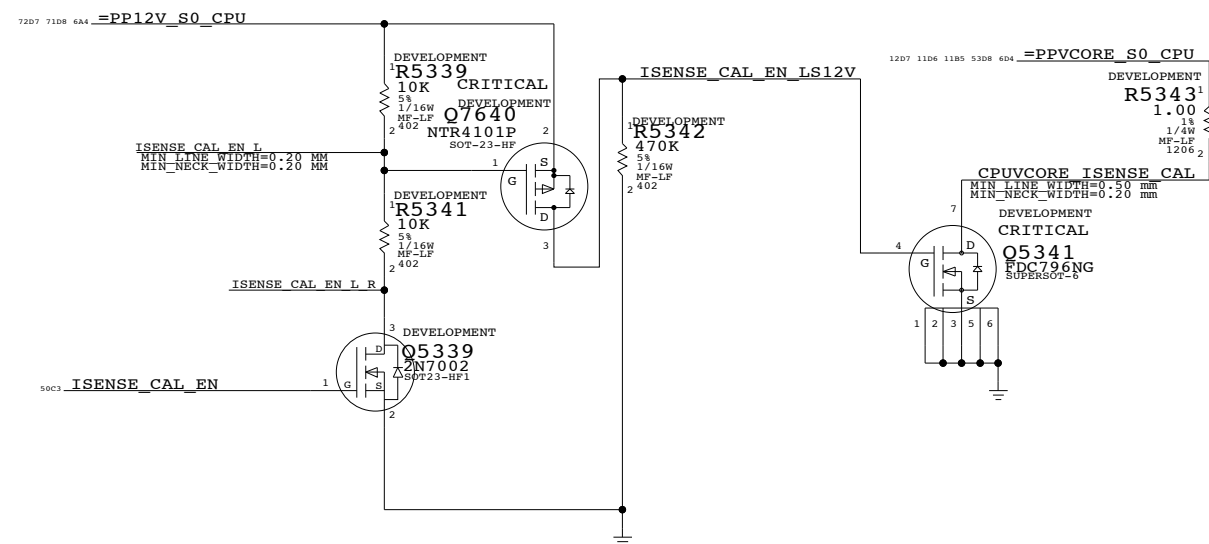
8	7	6	5	4	3	2	1
---	---	---	---	---	---	---	---







## CPU POWER SENSE CALIBRATION CIRCUIT



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION	RANGE
107S0069	1	10 MILLIOHM	R5382	CRITICAL	K50_BETTER	10A
107S0112	1	8 MILLIOHM	R5382	CRITICAL	24_INCH_MXM	12.5
107S0070	2	RES, 0 OHM, 2512	R5381, R5382	CRITICAL	IG	
107S0111	1	18 MILLIOHM	R5381	CRITICAL	12V_PWR_SENSE	5.5A
116S0090	2	RES, 10KOHM, 5%, 402	C5383, C5384		IG	
132S0080	2	CAP, 0.22UF, 20%, 6.3V, X5R, 402	C5383, C5384		12V_PWR_SENSE	


```

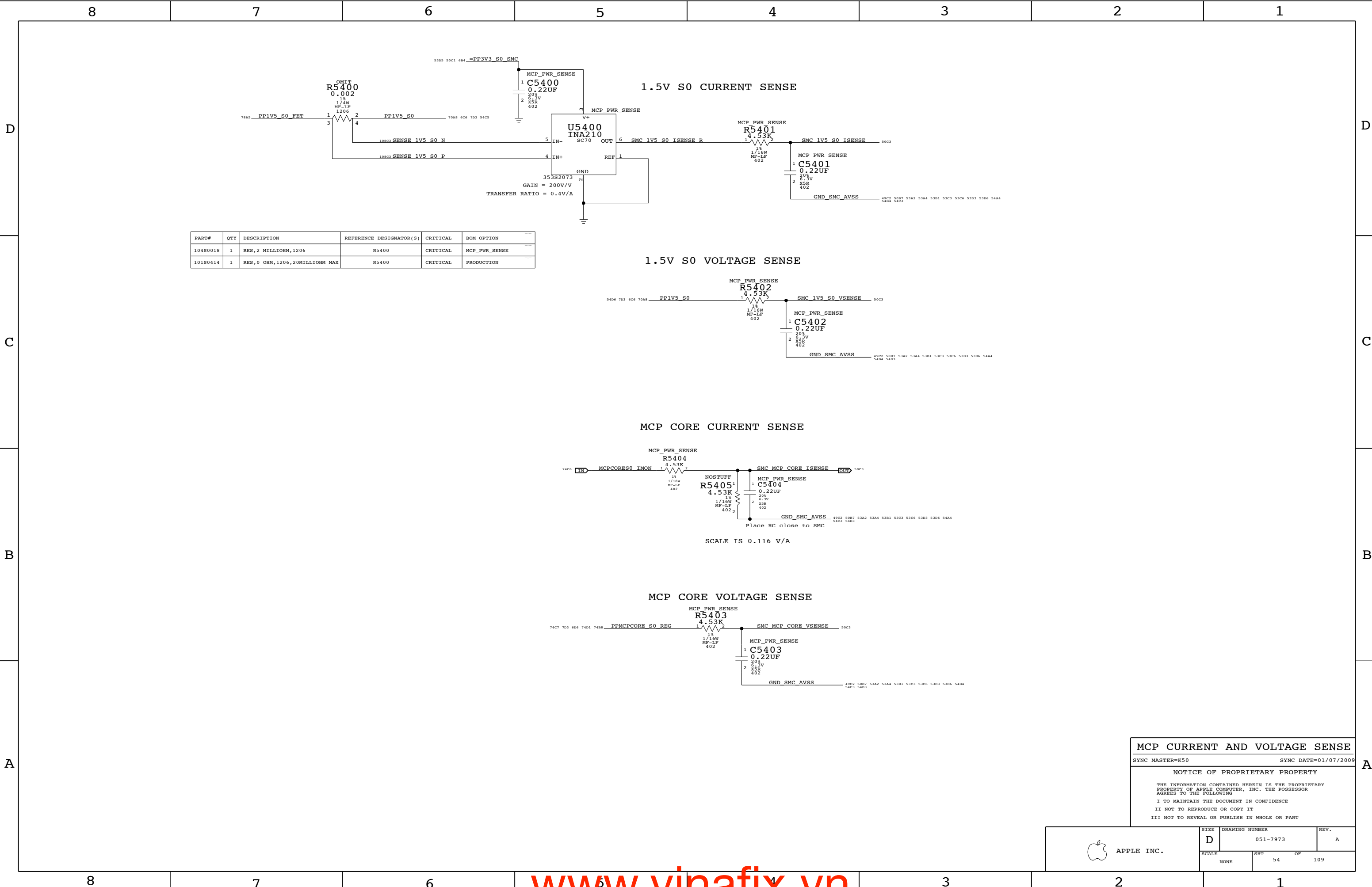
12V_PWR_SENSE SHOULD BE STUFFED FOR MMX CONFIGS
IG CONFIGS WILL NOT HAVE THE SENSORS, SO CAPS FROM THE RC FILTER
    BECOME RESISTORS TO GROUND (SO SMC READS 0)

IG CONFIGS DO NOT NEED 12V POWER SENSE BECAUSE THE CONFIGURATION DOES NOT DRAW
CURRENT WHICH APPROACHES THE ADCD SPEC

```

<h1>Current &amp; Voltage Sensing</h1>	
SYNC_MASTER=K50	SYNC_DATE=01/07/2009
<h2>NOTICE OF PROPRIETARY PROPERTY</h2>	
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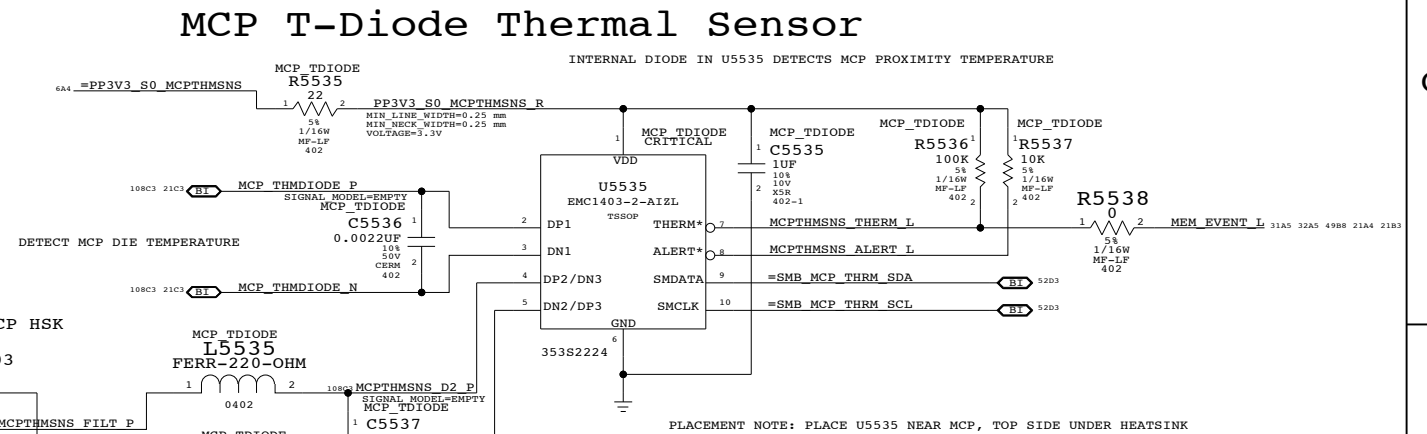
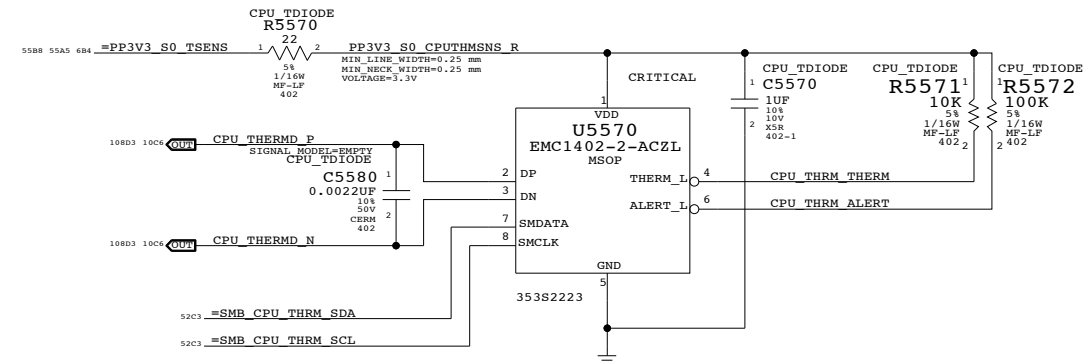
 APPLE INC.	SIZE <b>D</b>	DRAWING NUMBER 051-7973	REV. A
	SCALE NONE	SHT 53 OF 109	



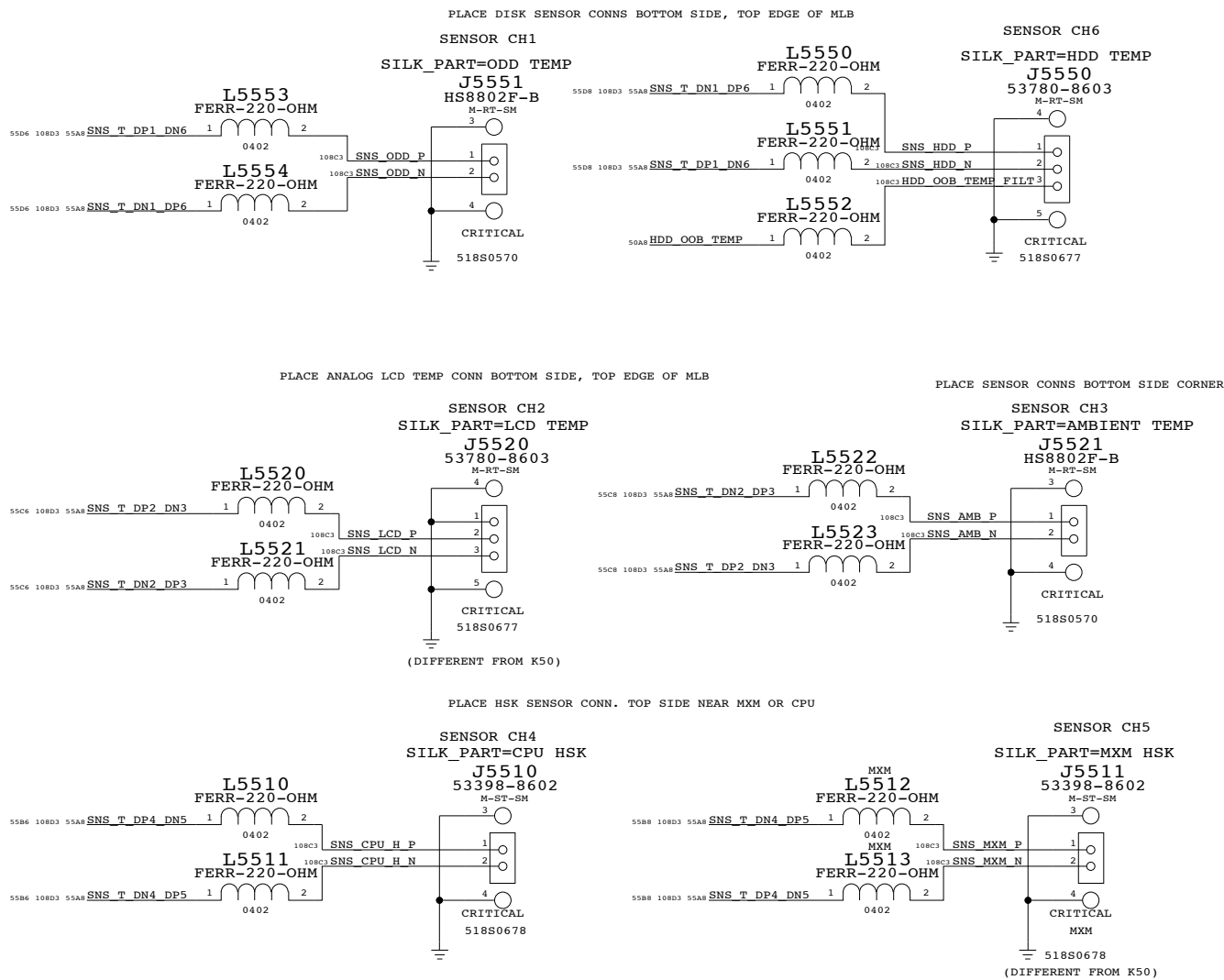
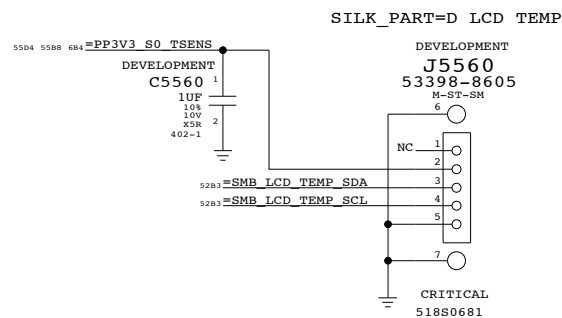


# REMOTE THERMAL SENSORS HEATSINKS, AMBIENT, PANEL AND DISKS

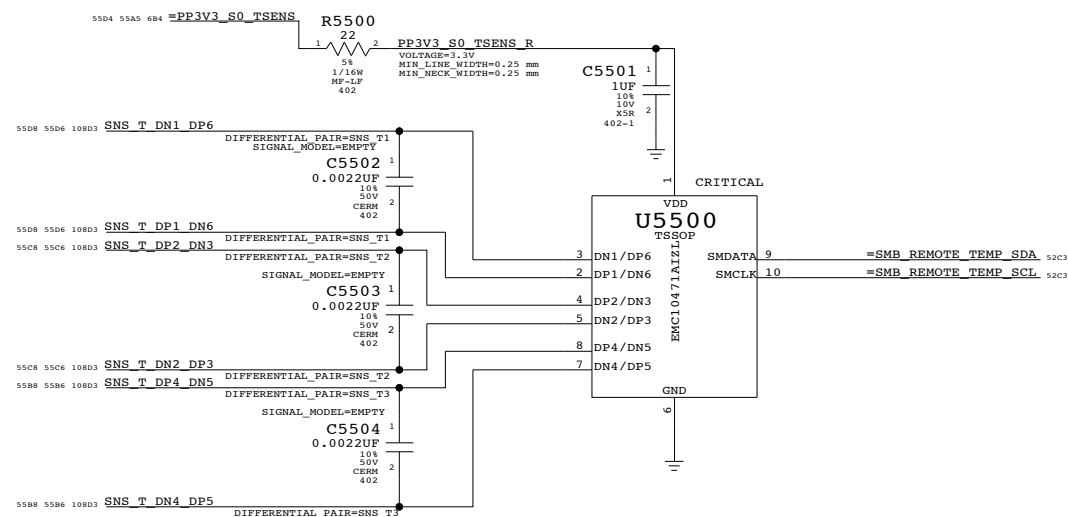
## CPU T-Diode Thermal Sensor



# DIGITAL LCD TEMP SENSOR



## REMOTE THERMAL SENSORS (HEATSINKS AND DISKS)



```

BROKE SYNC FROM K50 ON 7/9

Thermal Sensors

SYNC_MASTER=DEREK                                SYNC_DATE=11/07/2008

NOTICE OF PROPRIETARY PROPERTY

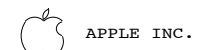
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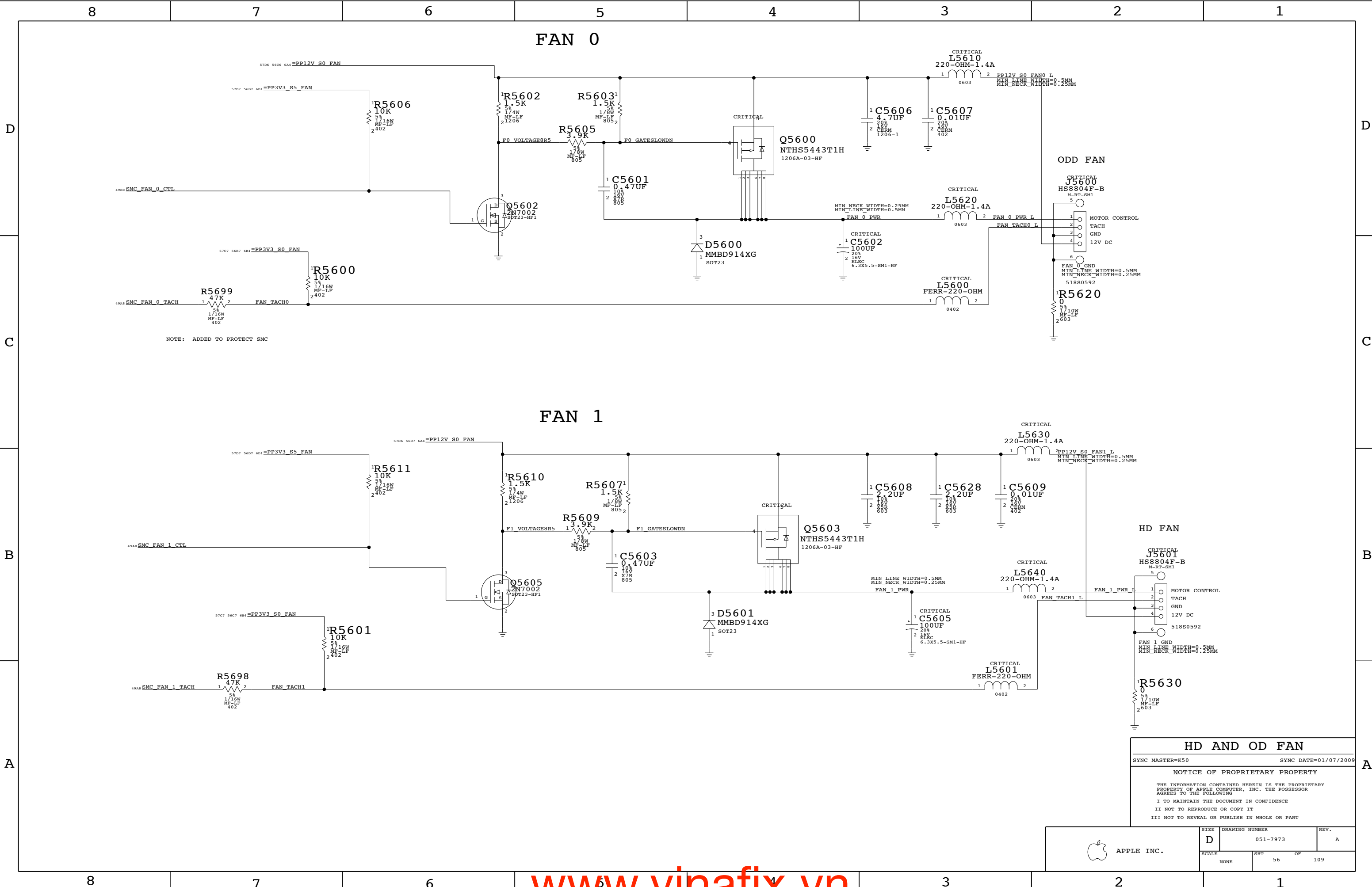
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HD AND OD FAN

SYNC\_MASTER=K50 SYNC\_DATE=01/07/2009

NOTICE OF PROPRIETARY PROPERTY

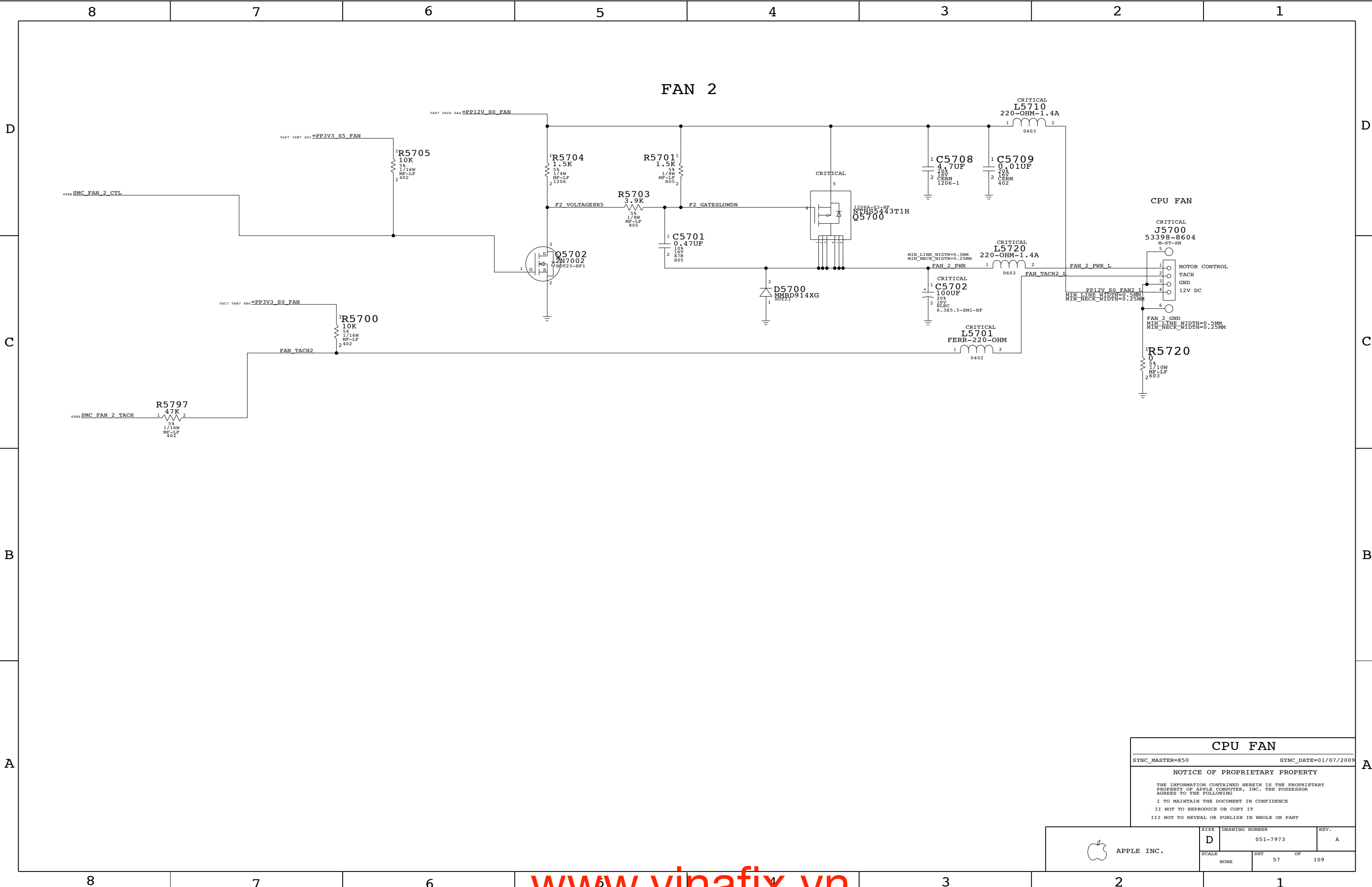
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7973	A
SCALE		SHT	OF
NONE		56	109



CPU FAN

SYNC\_MASTER=K50

SYNC\_DATE=01/07/2009

NOTICE OF PROPRIETARY PROPERTY

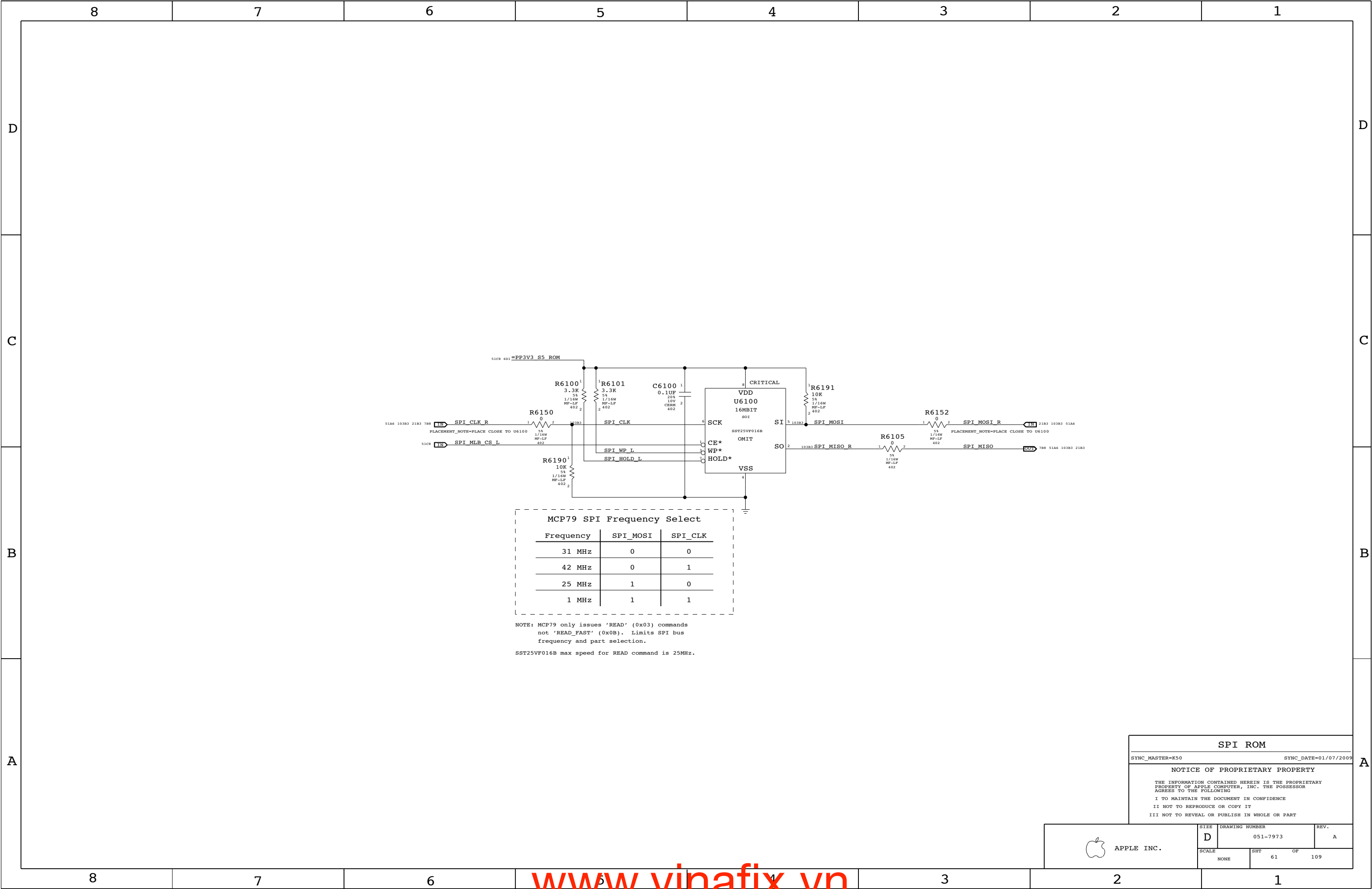
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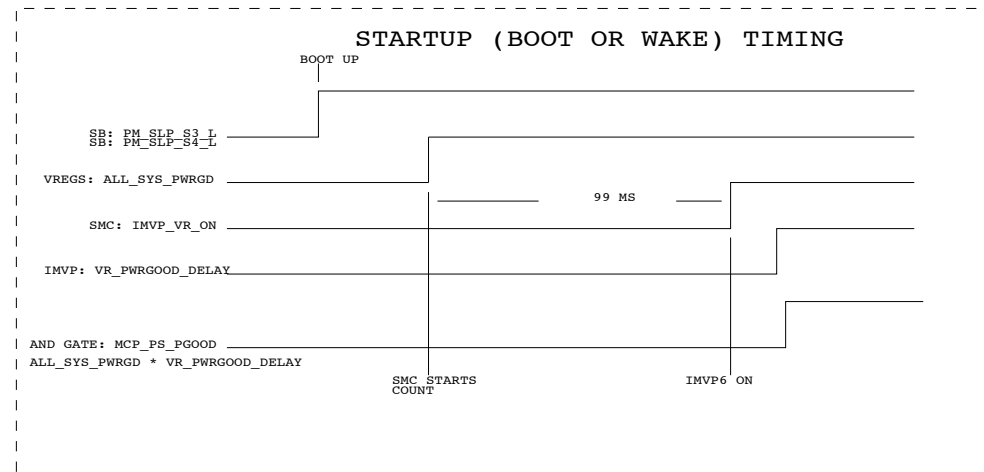
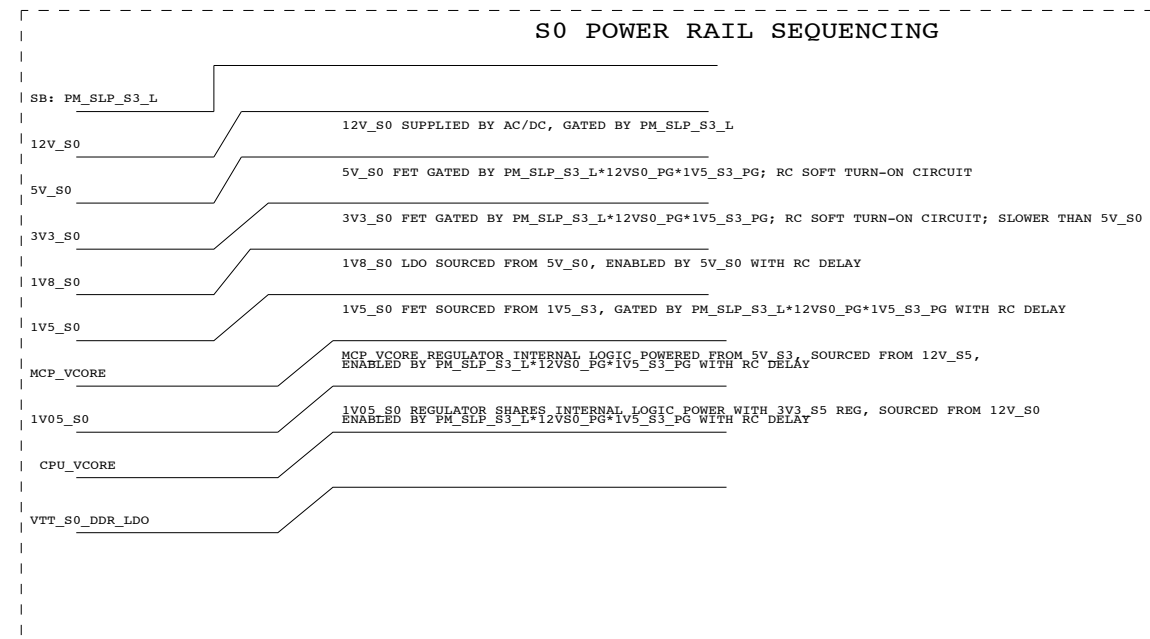
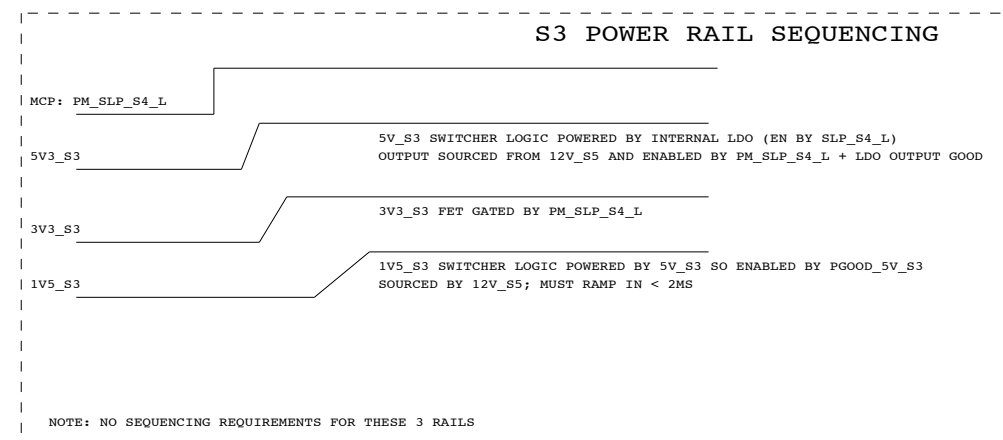
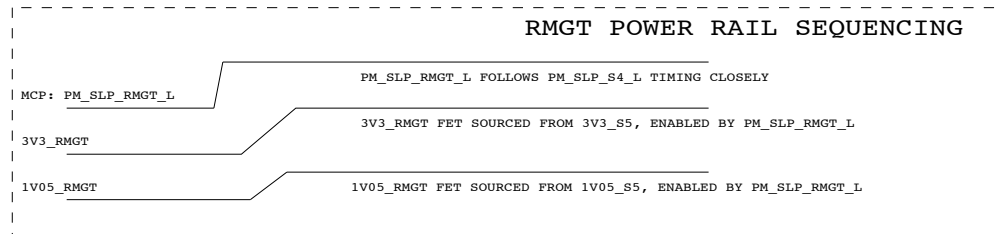
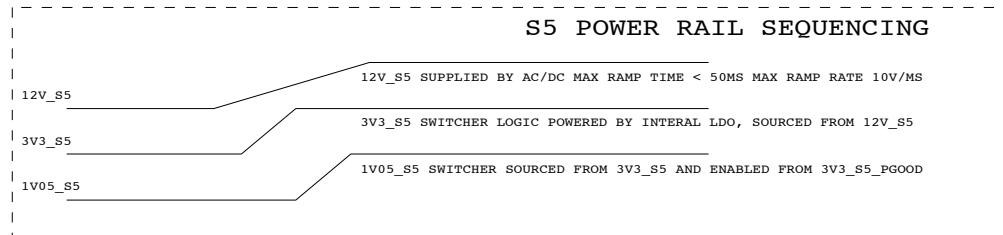
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7973	A
SCALE		SHT	OF
NONE		57	109

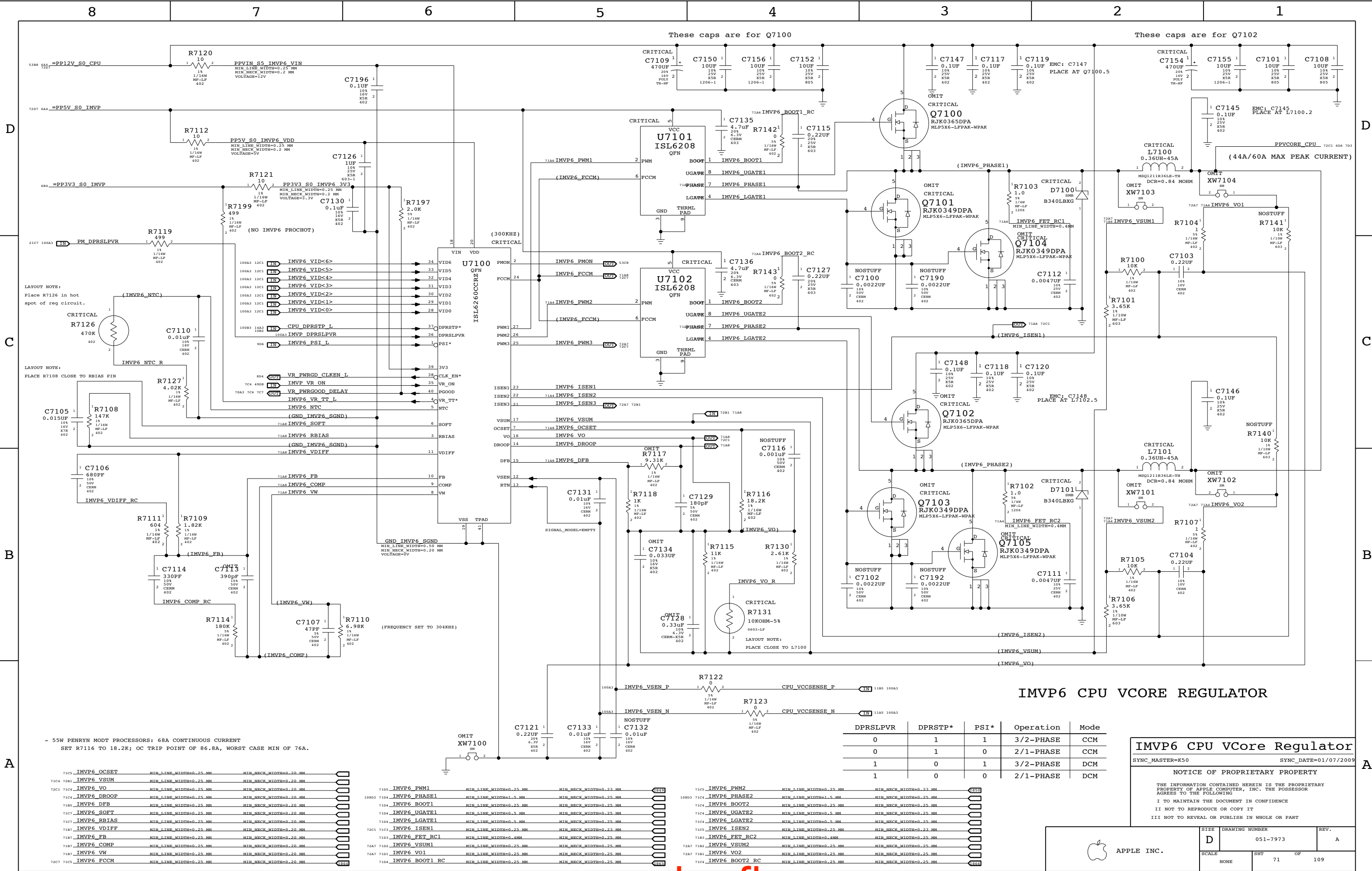




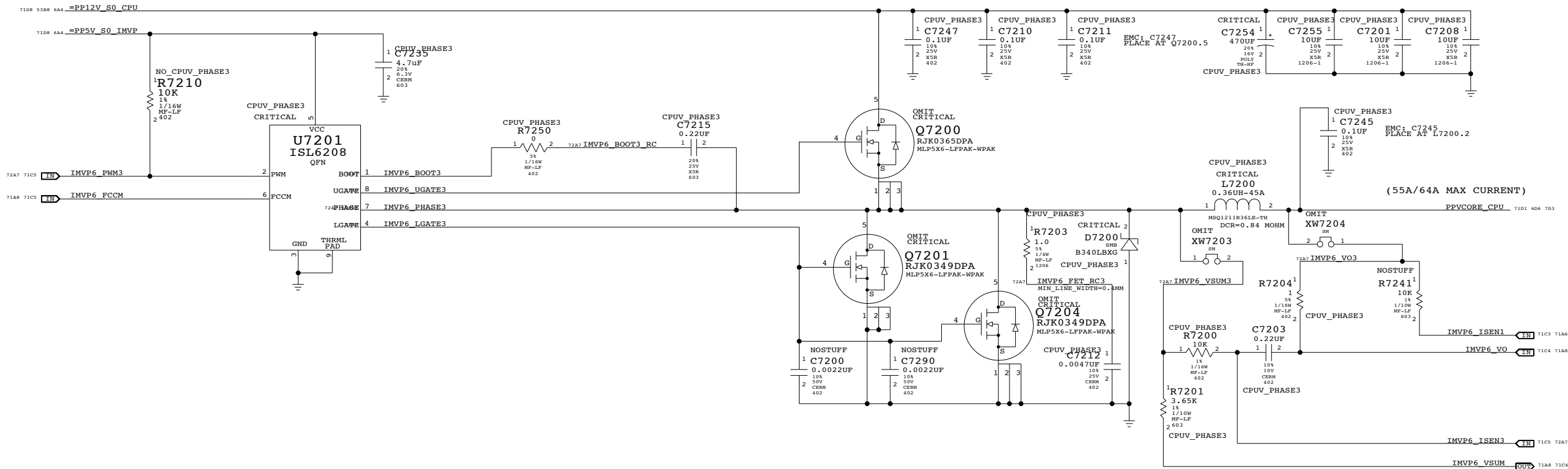
State	Manageability	SMC_PM_G2_ENABLE	PM_S4_STATE_L	PM_SLP_S3_L	PM_SLP_S4_L	PM_SLP_M_L
Run (S0/M0)	N/A	1	1	1	1	1
Sleep (S3/M1)	On	1	1	0	1	1
Soft-Off (S5/M1)	On	1	0	0	1	1
Sleep (S3/M-Off)	Off	1	1	0	1	0
Soft-Off (S5/M-Off)	Off	1	0	0	0	0
Battery Off (G3Hot)	N/A	0	0	0	0	0







IMVP6 CPU VCORE REGULATOR



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
376S0693	6	RENESAS BOT FET	Q7101,Q7103,Q7104,Q7105,Q7201,Q7204	RENESAS_FET
376S0733	6	TOSHIBA BOT FET	Q7101,Q7103,Q7104,Q7105,Q7201,Q7204	TOSHIBA_FET
376S0694	3	RENASAS TOP FET	Q7100,Q7102,Q7200	RENESAS_FET
376S0732	3	TOSHIBA TOP FET	Q7100,Q7102,Q7200	TOSHIBA_FET

NO TEST FOR CPU VREG, ADDED K2/K3

71A6 7101	IMVP6_VO1	NO_TEST=TRUE
71A4 7181	IMVP6_VO2	NO_TEST=TRUE
72A7 72C7	IMVP6_VO3	NO_TEST=TRUE
71A6 7102	IMVP6_VSUM1	NO_TEST=TRUE
71A4 7182	IMVP6_VSUM2	NO_TEST=TRUE
72A7 72C3	IMVP6_VSUM3	NO_TEST=TRUE

72C7 71C5	IMVP6_PWM3	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.23 MM	151
10B03 72C4	IMVP6_PHASE3	MIN_LINE_WIDTH=1.5 MM	MIN_NECK_WIDTH=0.25 MM	149
72C4	IMVP6_BOOT3	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM	149
72C4	IMVP6_UGATE3	MIN_LINE_WIDTH=0.5 MM	MIN_NECK_WIDTH=0.25 MM	149
72C4	IMVP6_LGATE3	MIN_LINE_WIDTH=0.5 MM	MIN_NECK_WIDTH=0.25 MM	149
72B1 71C5	IMVP6_ISEN3	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.23 MM	149
72C3	IMVP6_FET_RC3	MIN_LINE_WIDTH=0.4MM	MIN_NECK_WIDTH=0.25 MM	149
72A7 72C3	IMVP6_VSUM3	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM	149
72A7 72C7	IMVP6_VO3	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM	150
72C5	IMVP6_BOOT3_RC	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM	151

IMVP6 3RD PHASE

SYNC\_MASTER=K50 SYNC\_DATE=01/07/2009

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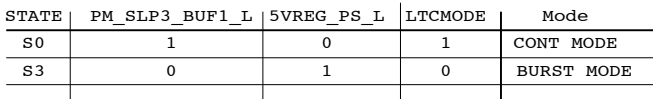
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SIZE D DRAWING NUMBER 051-7973 REV. A

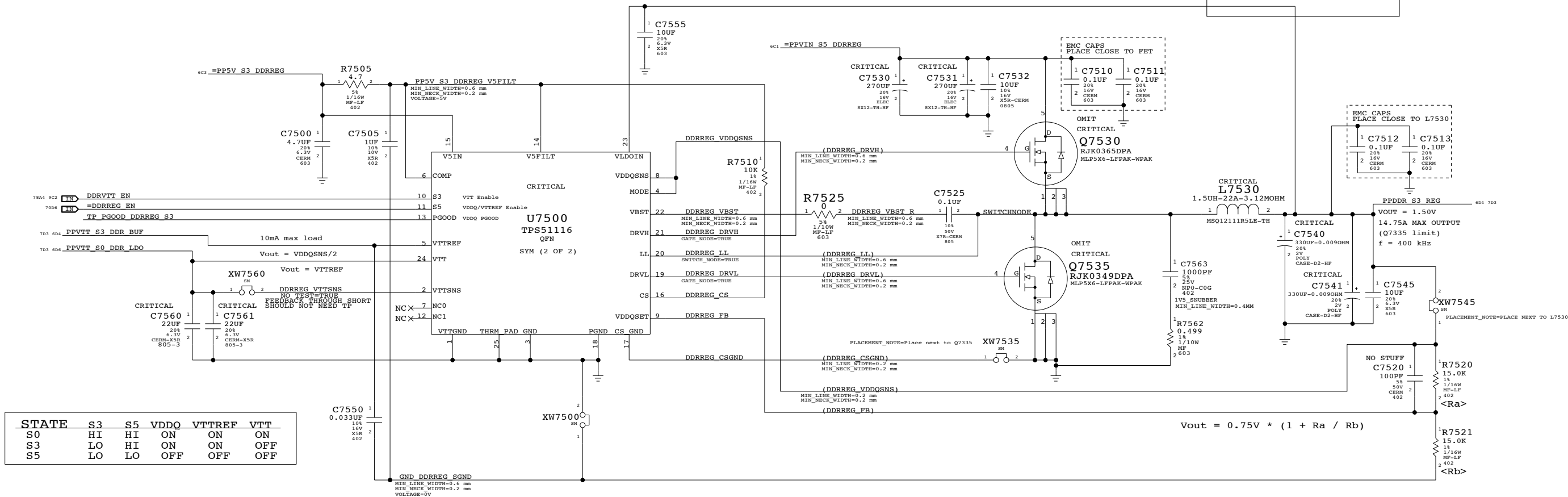
SCALE NONE SHT 72 OF 109

[illegible]

 APPLE INC.	SIZE <b>D</b>	DRAWING NUMBER 051-7973	REV. A
	SCALE NONE	SHT                      OF 73                      109	



# 1.5 V DDR SUPPLY



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
376S0693	1	RENESAS BOT FET	Q7535	RENESAS_FET
376S0733	1	TOSHIBA BOT FET	Q7535	TOSHIBA_FET
376S0694	1	RENASAS TOP FET	Q7530	RENESAS_FET
376S0732	1	TOSHIBA TOP FET	Q7530	TOSHIBA_FET

## 1.5V DDR SUPPLY

SYNC\_MASTER=K50 SYNC\_DATE=01/07/2009

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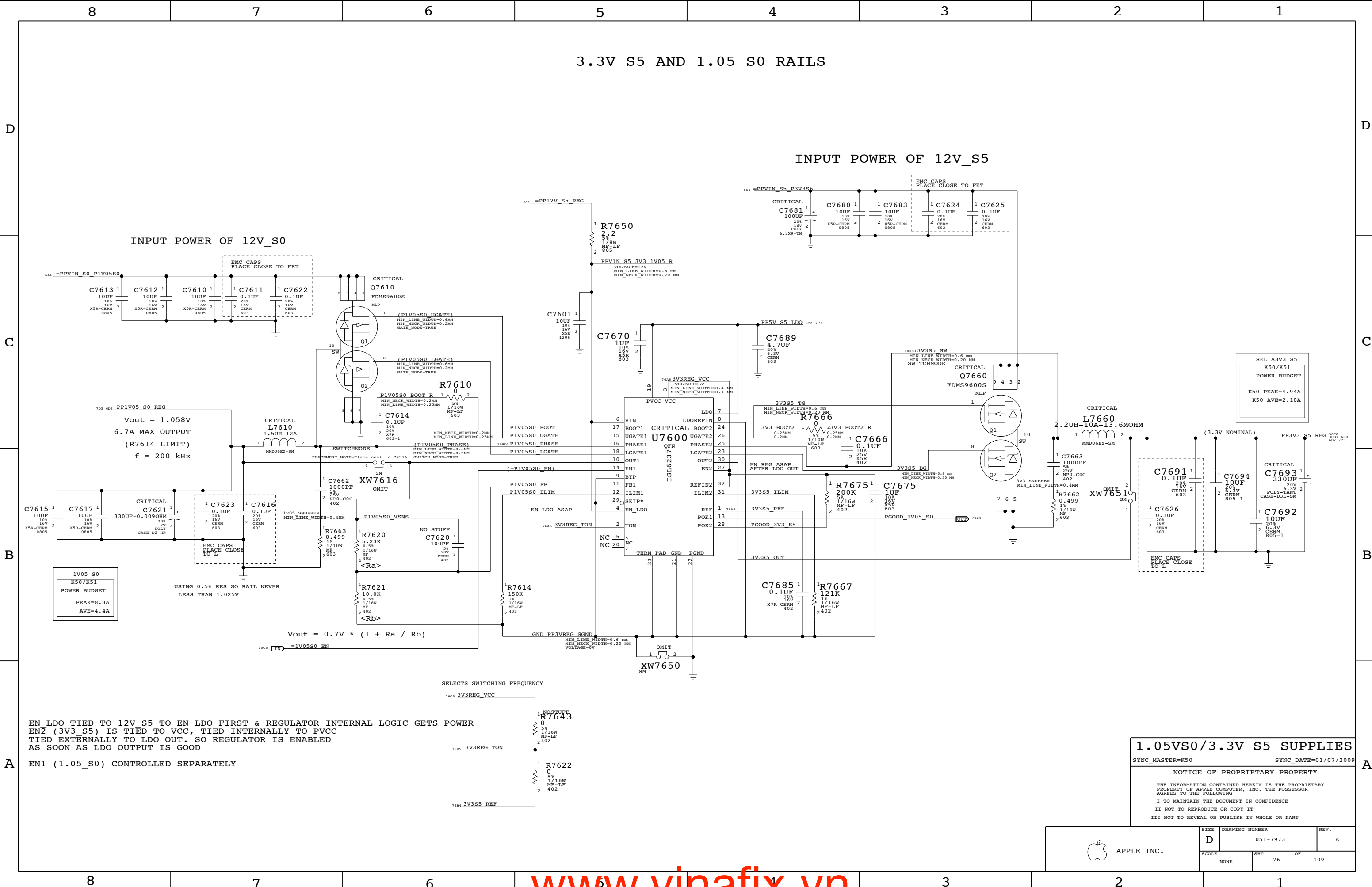
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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7973	A
SCALE	SHT	OF
NONE	75	109



3.3V S5 AND 1.05 S0 RAILS

INPUT POWER OF 12V\_S5

INPUT POWER OF 12V\_S0

1.05VS0/3.3V S5 SUPPLIES

SYNC\_MASTER=K50 SYNC\_DATE=01/07/2009

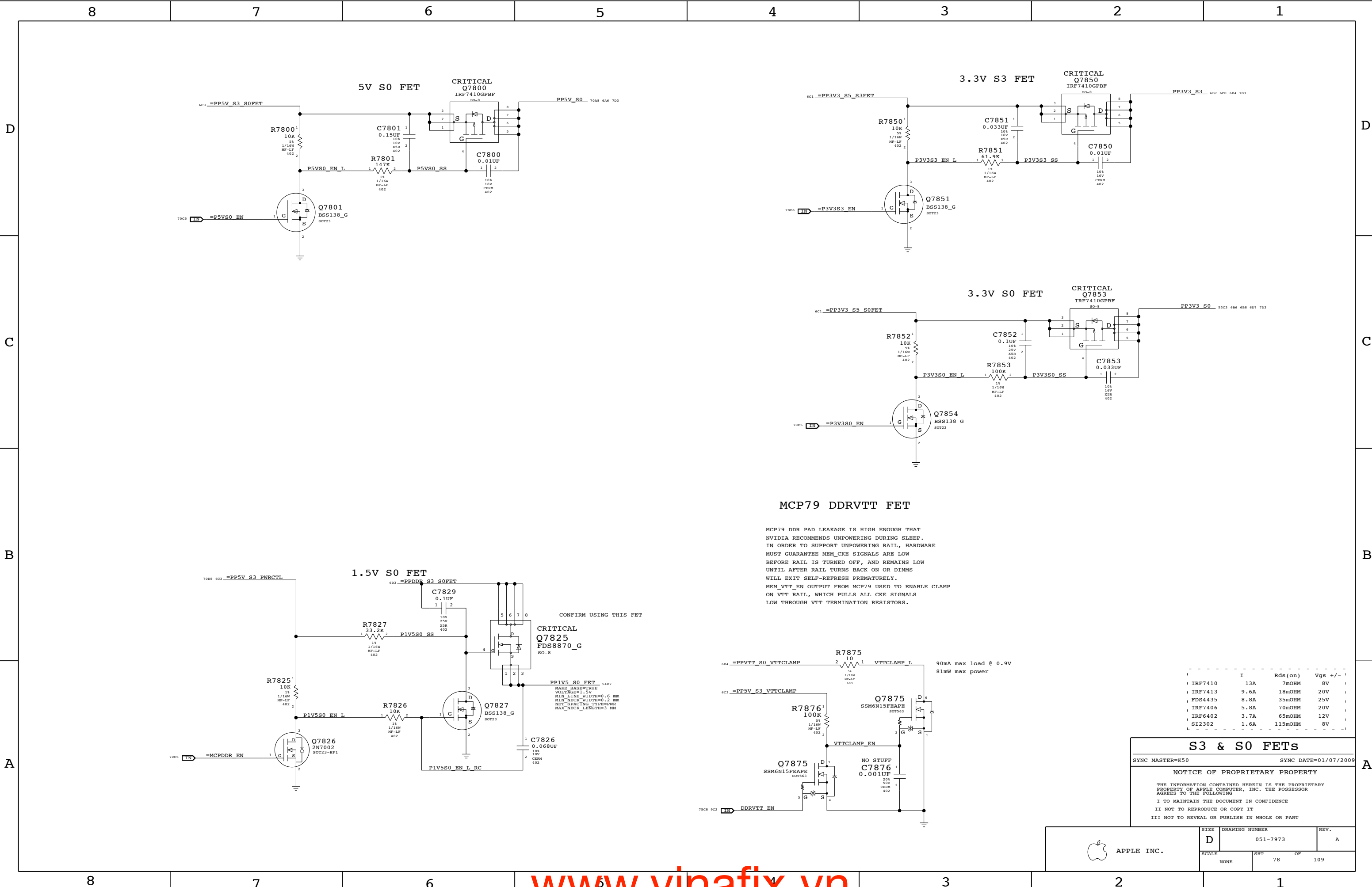
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SIZE	DRAWING NUMBER	REV.
D	051-7973	A
SCALE	SHT	OF
NONE	76	109





MCP79 DDRVTT FET

MCP79 DDR PAD LEAKAGE IS HIGH ENOUGH THAT NVIDIA RECOMMENDS UNPOWERING DURING SLEEP. IN ORDER TO SUPPORT UNPOWERING RAIL, HARDWARE MUST GUARANTEE MEM\_CKE SIGNALS ARE LOW BEFORE RAIL IS TURNED OFF, AND REMAINS LOW UNTIL AFTER RAIL TURNS BACK ON OR DIMMS WILL EXIT SELF-REFRESH PREMATURELY. MEM\_VTT\_EN OUTPUT FROM MCP79 USED TO ENABLE CLAMP ON VTT RAIL, WHICH PULLS ALL CKE SIGNALS LOW THROUGH VTT TERMINATION RESISTORS.

	I	Rds (on)	Vgs +/-
IRF7410	13A	7mOHM	8V
IRF7413	9.6A	18mOHM	20V
FDS4435	8.8A	35mOHM	25V
IRF7406	5.8A	70mOHM	20V
IRF6402	3.7A	65mOHM	12V
SI2302	1.6A	115mOHM	8V

S3 & S0 FETs

SYNC\_MASTER=K50 SYNC\_DATE=01/07/2009

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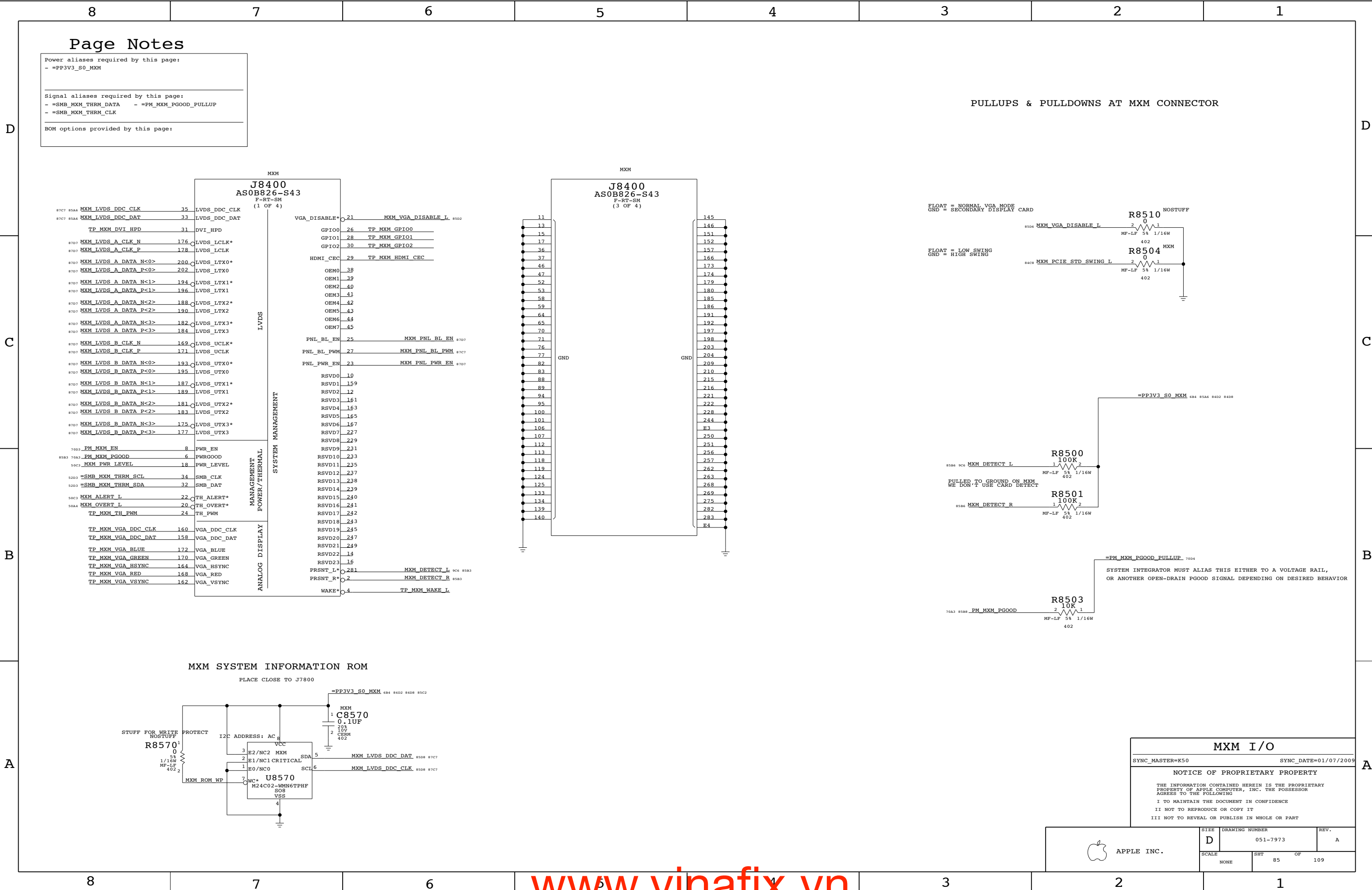
SIZE	DRAWING NUMBER	REV.
D	051-7973	A
SCALE	SHT	OF
NONE	78	109











8	7	6	5	4	3	2	1
SLOTB MXM TX CAPS				SLOTB MXM RX CAPS			
D	102D3 9C6	102D3 9C6	102D3 9C6	102D3 9C6	102D3 9C6	102D3 9C6	102D3 9C6
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	102D3 9C6	102D3 9C6	102D3 9C6	102D3 9C6	102D3 9C6	102D3 9C6	102D3 9C6
	102D3 9C6	102D3 9C6	102D3 9C6	102D3 9C6	102D3 9C6	102D3 9C6	102D3 9C6
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	102D3 9C6	102D3 9C6	102D3 9C6	102D3 9C6	102D3 9C6	102D3 9C6	102D3 9C6
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	102D3 9C6	102D3 9C6	102D3 9C6	102D3 9C6	102D3 9C6	102D3 9C6	102D3 9C6
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	102D3 9C6	102D3 9C6	102D3 9C6	102D3 9C6	102D3 9C6	102D3 9C6	102D3 9C6
A	102D3 9C6	102D3 9C6	102D3 9C6	102D3 9C6	102D3 9C6	102D3 9C6	102D3 9C6
	102D3 9C6	102D3 9C6	102D3 9C6	102D3 9C6	102D3 9C6	102D3 9C6	102D3 9C6
	102D3 9C6	102D3 9C6	102D3 9C6	102D3 9C6	102D3 9C6	102D3 9C6	102D3 9C6
	102D3 9C6	102D3 9C6	102D3 9C6	102D3 9C6	102D3 9C6	102D3 9C6	102D3 9C6
	102D3 9C6	102D3 9C6	102D3 9C6	102D3 9C6	102D3 9C6	102D3 9C6	102D3 9C6
	102D3 9C6	102D3 9C6	102D3 9C6	102D3 9C6	102D3 9C6	102D3 9C6	102D3 9C6
	102D3 9C6	102D3 9C6	102D3 9C6	102D3 9C6	102D3 9C6	102D3 9C6	102D3 9C6
	102D3 9C6	102D3 9C6	102D3 9C6	102D3 9C6	102D3 9C6	102D3 9C6	102D3 9C6
	102D3 9C6	102D3 9C6	102D3 9C6	102D3 9C6	102D3 9C6	102D3 9C6	102D3 9C6
	102D3 9C6	102D3 9C6	102D3 9C6	102D3 9C6	102D3 9C6	102D3 9C6	102D3 9C6

MXM PCIE CAPS

SYNC\_MASTER=K50

SYNC\_DATE=01/07/2009

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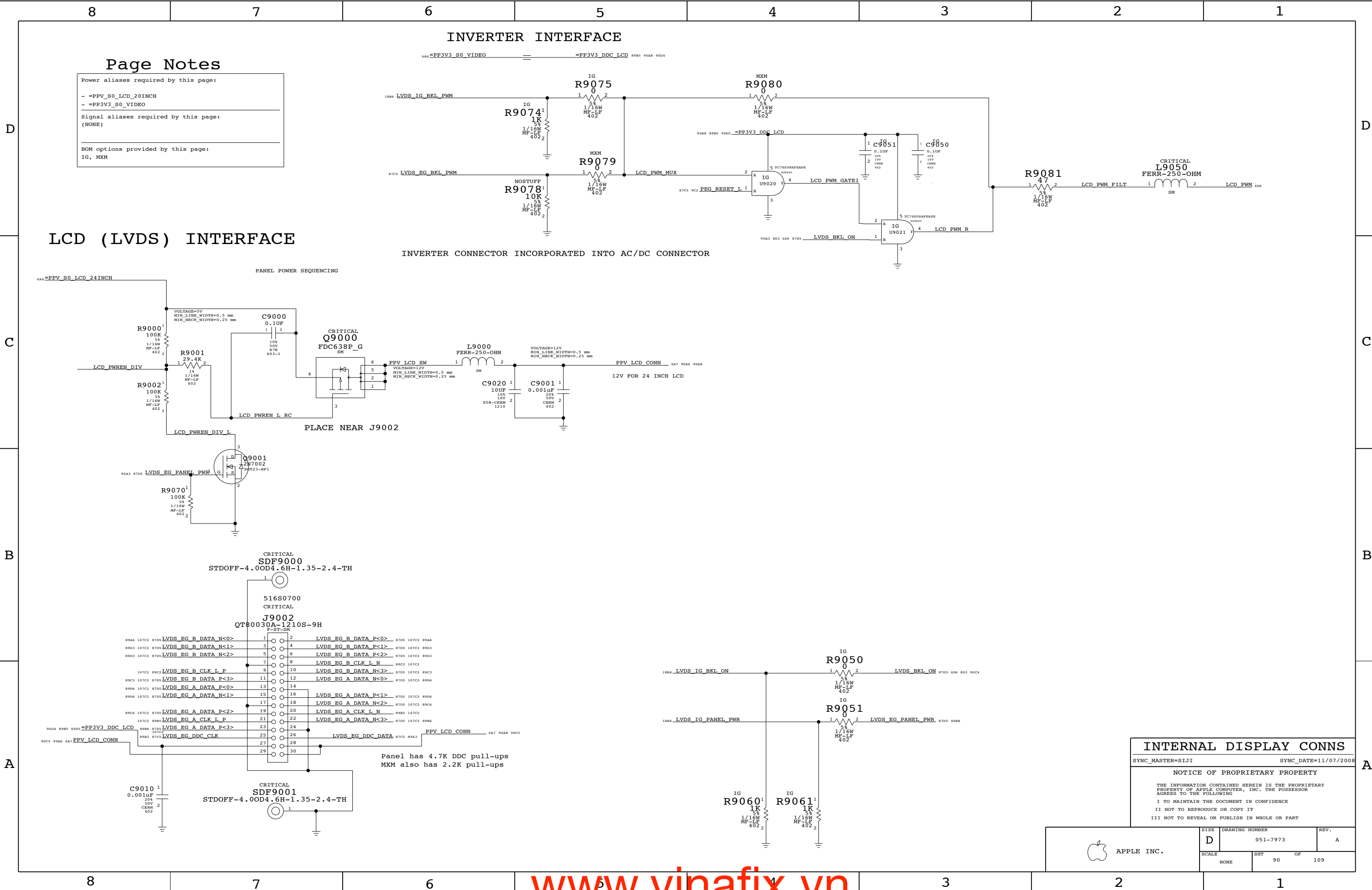
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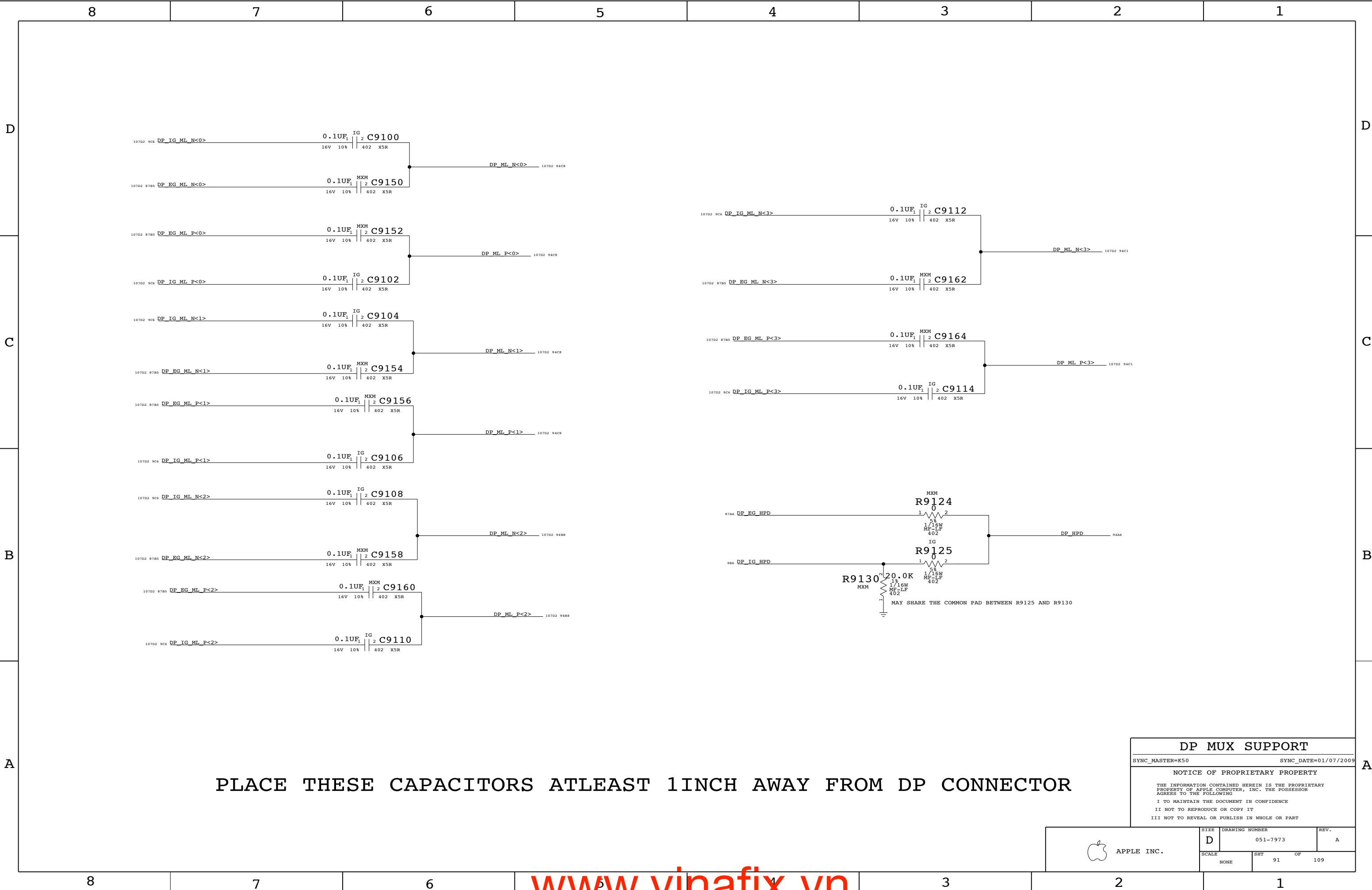
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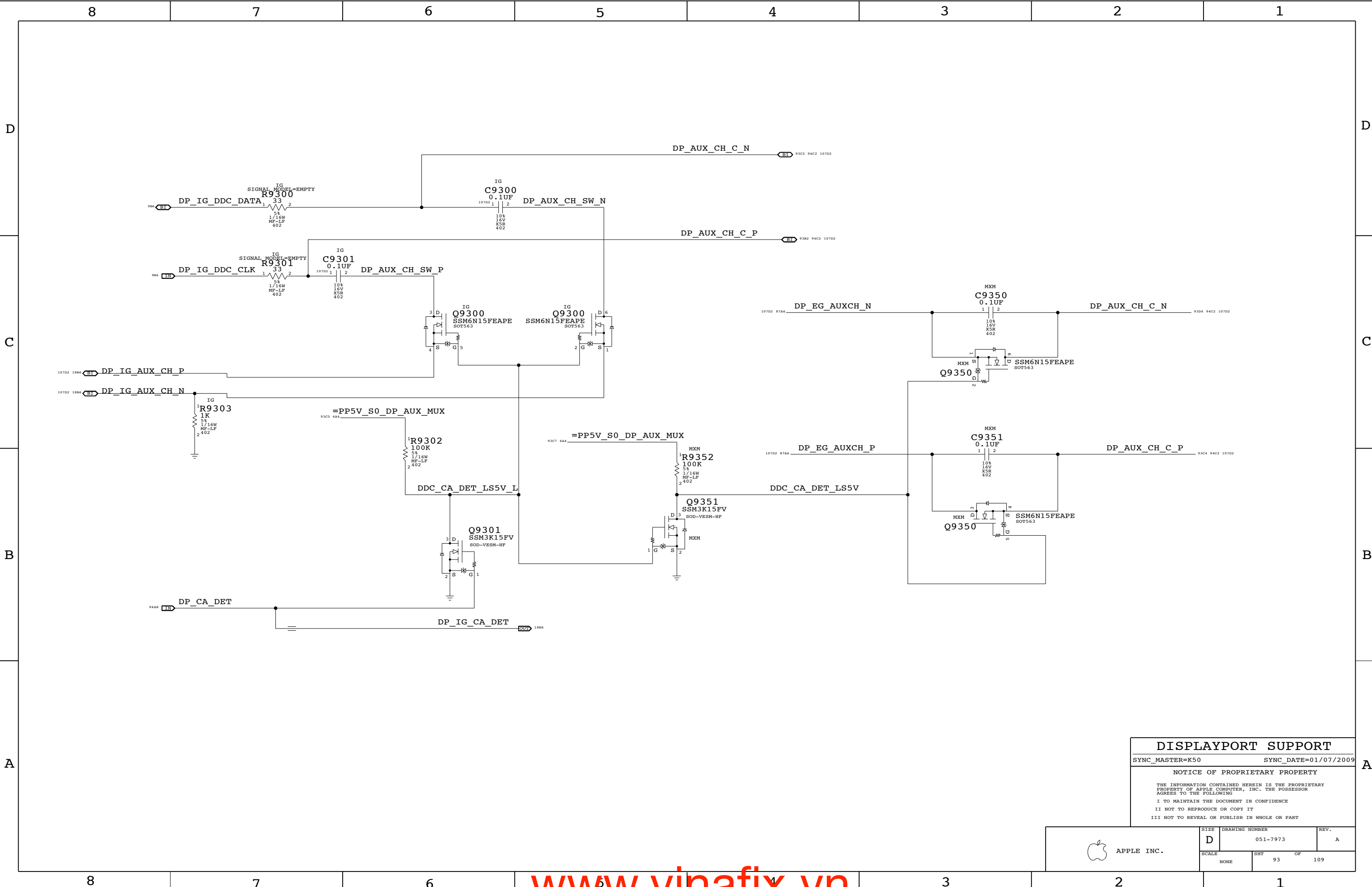
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<div><div>Page Notes</div><div><div>Power aliases required by this page: - =PP5V_DP_AUX</div><div>Signal aliases required by this page: (NONE)</div><div>BOM options provided by this page: (NONE)</div></div></div>																<div><div>UNUSED DP INTERFACES</div><div><div><div>84B5</div><div>MXM_DP_C_ML_N&lt;0..3&gt;</div><div>==</div><div>TP_MXM_DP_C_ML_N&lt;0..3&gt;</div><div>MAKE_BASE=TRUE</div></div><div><div>84B5</div><div>MXM_DP_C_ML_P&lt;0..3&gt;</div><div>==</div><div>TP_MXM_DP_C_ML_P&lt;0..3&gt;</div><div>MAKE_BASE=TRUE</div></div><div><div>84C5</div><div>MXM_DP_C_AUX_N</div><div>==</div><div>TP_MXM_DP_C_AUX_N</div><div>MAKE_BASE=TRUE</div></div><div><div>84C5</div><div>MXM_DP_C_AUX_P</div><div>==</div><div>TP_MXM_DP_C_AUX_P</div><div>MAKE_BASE=TRUE</div></div><div><div>84B5</div><div>MXM_DP_C_HPD</div><div>==</div><div>TP_MXM_DP_C_HPD</div><div>MAKE_BASE=TRUE</div></div></div></div>															
<div><div>MXM</div><div><div>84C5</div><div>MXM_DP_A_ML_N&lt;0&gt;</div><div>==</div><div>DP_EG_ML_N&lt;0&gt;</div><div>MAKE_BASE=TRUE</div><div>107D2 91D8</div></div><div><div>84C5</div><div>MXM_DP_A_ML_P&lt;0&gt;</div><div>==</div><div>DP_EG_ML_P&lt;0&gt;</div><div>MAKE_BASE=TRUE</div><div>107D2 91C8</div></div><div><div>84C5</div><div>MXM_DP_A_ML_N&lt;1&gt;</div><div>==</div><div>DP_EG_ML_N&lt;1&gt;</div><div>MAKE_BASE=TRUE</div><div>107D2 91C8</div></div><div><div>84C5</div><div>MXM_DP_A_ML_P&lt;1&gt;</div><div>==</div><div>DP_EG_ML_P&lt;1&gt;</div><div>MAKE_BASE=TRUE</div><div>107D2 91C8</div></div><div><div>84C5</div><div>MXM_DP_A_ML_N&lt;2&gt;</div><div>==</div><div>DP_EG_ML_N&lt;2&gt;</div><div>MAKE_BASE=TRUE</div><div>107D2 91B8</div></div><div><div>84C5</div><div>MXM_DP_A_ML_P&lt;2&gt;</div><div>==</div><div>DP_EG_ML_P&lt;2&gt;</div><div>MAKE_BASE=TRUE</div><div>107D2 91B7</div></div><div><div>84C5</div><div>MXM_DP_A_ML_N&lt;3&gt;</div><div>==</div><div>DP_EG_ML_N&lt;3&gt;</div><div>MAKE_BASE=TRUE</div><div>107D2 91C4</div></div><div><div>84C5</div><div>MXM_DP_A_ML_P&lt;3&gt;</div><div>==</div><div>DP_EG_ML_P&lt;3&gt;</div><div>MAKE_BASE=TRUE</div><div>107D2 91C4</div></div><div><div>84C5</div><div>MXM_DP_A_HPD</div><div>==</div><div>DP_EG_HPD</div><div>MAKE_BASE=TRUE</div><div>91B4</div></div><div><div>84D5</div><div>MXM_DP_A_AUX_N</div><div>==</div><div>DP_EG_AUXCH_N</div><div>MAKE_BASE=TRUE</div><div>93C4 107D2</div></div><div><div>84C5</div><div>MXM_DP_A_AUX_P</div><div>==</div><div>DP_EG_AUXCH_P</div><div>MAKE_BASE=TRUE</div><div>93B4 107D2</div></div></div>																<div><div>EXTERNAL DP CONN</div><div>THESE ALIASES ARE TO CONFORM WITH K50/K52 SHARED CONNECTOR PAGE</div><div><div>84B5</div><div>MXM_DP_D_ML_N&lt;0..3&gt;</div><div>==</div><div>TP_MXM_DP_D_ML_N&lt;0..3&gt;</div><div>MAKE_BASE=TRUE</div></div><div><div>84B5</div><div>MXM_DP_D_ML_P&lt;0..3&gt;</div><div>==</div><div>TP_MXM_DP_D_ML_P&lt;0..3&gt;</div><div>MAKE_BASE=TRUE</div></div><div><div>84B5</div><div>MXM_DP_D_AUX_N</div><div>==</div><div>TP_MXM_DP_D_AUX_N</div><div>MAKE_BASE=TRUE</div></div><div><div>84B5</div><div>MXM_DP_D_AUX_P</div><div>==</div><div>TP_MXM_DP_D_AUX_P</div><div>MAKE_BASE=TRUE</div></div><div><div>84B5</div><div>MXM_DP_D_HPD</div><div>==</div><div>TP_MXM_DP_D_HPD</div><div>MAKE_BASE=TRUE</div></div></div>															
<div><div>MXM ALIASES</div><div><div>SYNC_MASTER=K50</div><div>SYNC_DATE=01/07/2009</div></div><div>NOTICE OF PROPRIETARY PROPERTY</div><div>THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING</div><div>I TO MAINTAIN THE DOCUMENT IN CONFIDENCE</div><div>II NOT TO REPRODUCE OR COPY IT</div><div>III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART</div></div>																<div><div><div><div>APPLE INC.</div></div><div><div>SCALE</div><div>NONE</div></div></div><div><div><div>SIZE</div><div>D</div></div><div><div>DRAWING NUMBER</div><div>051-7973</div></div><div><div>REV.</div><div>A</div></div></div><div><div><div>SHT</div><div>87</div><div>OF</div><div>109</div></div></div></div>															
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DISPLAYPORT SUPPORT

SYNC\_MASTER=K50

SYNC\_DATE=01/07/2009

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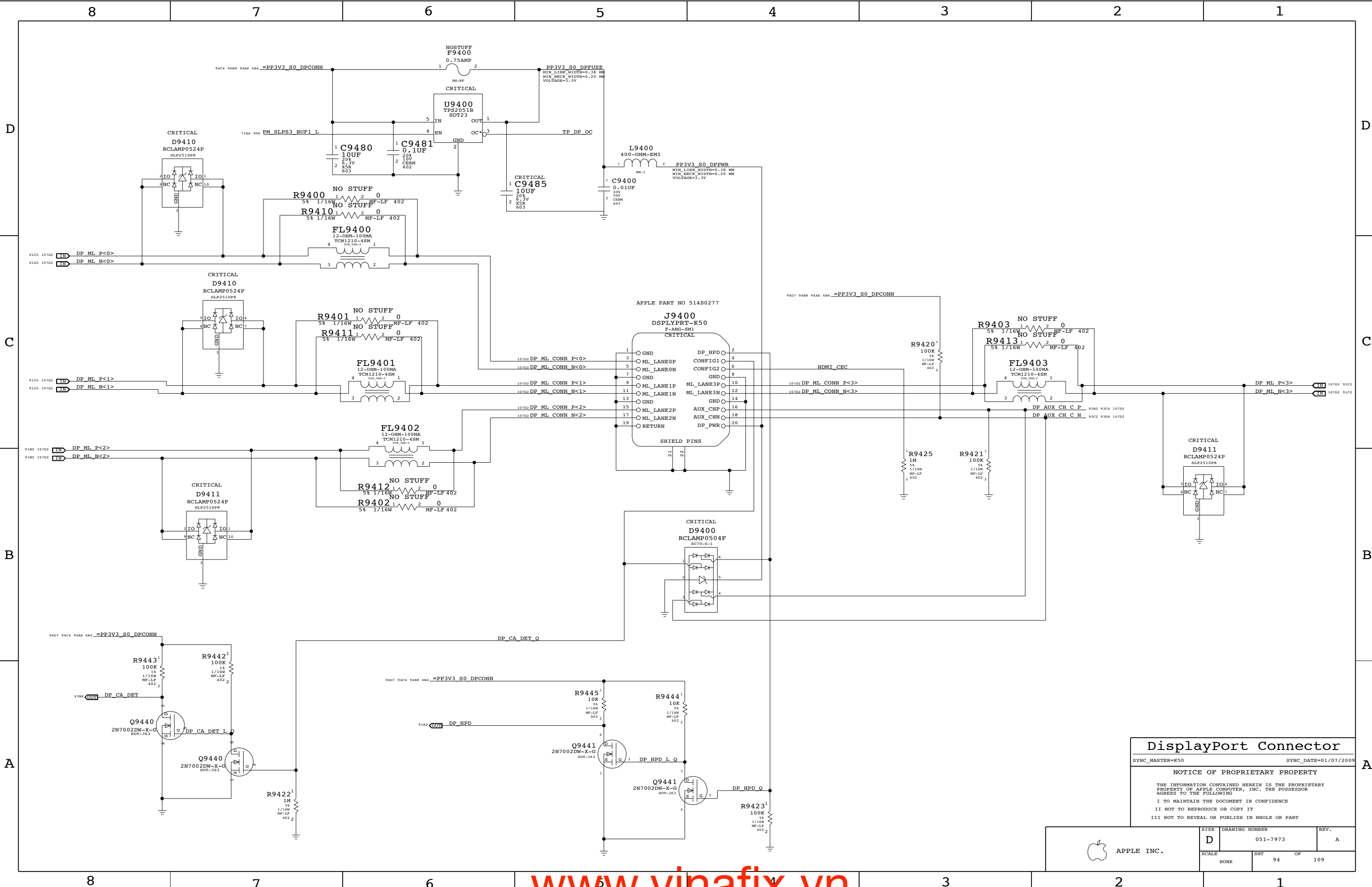
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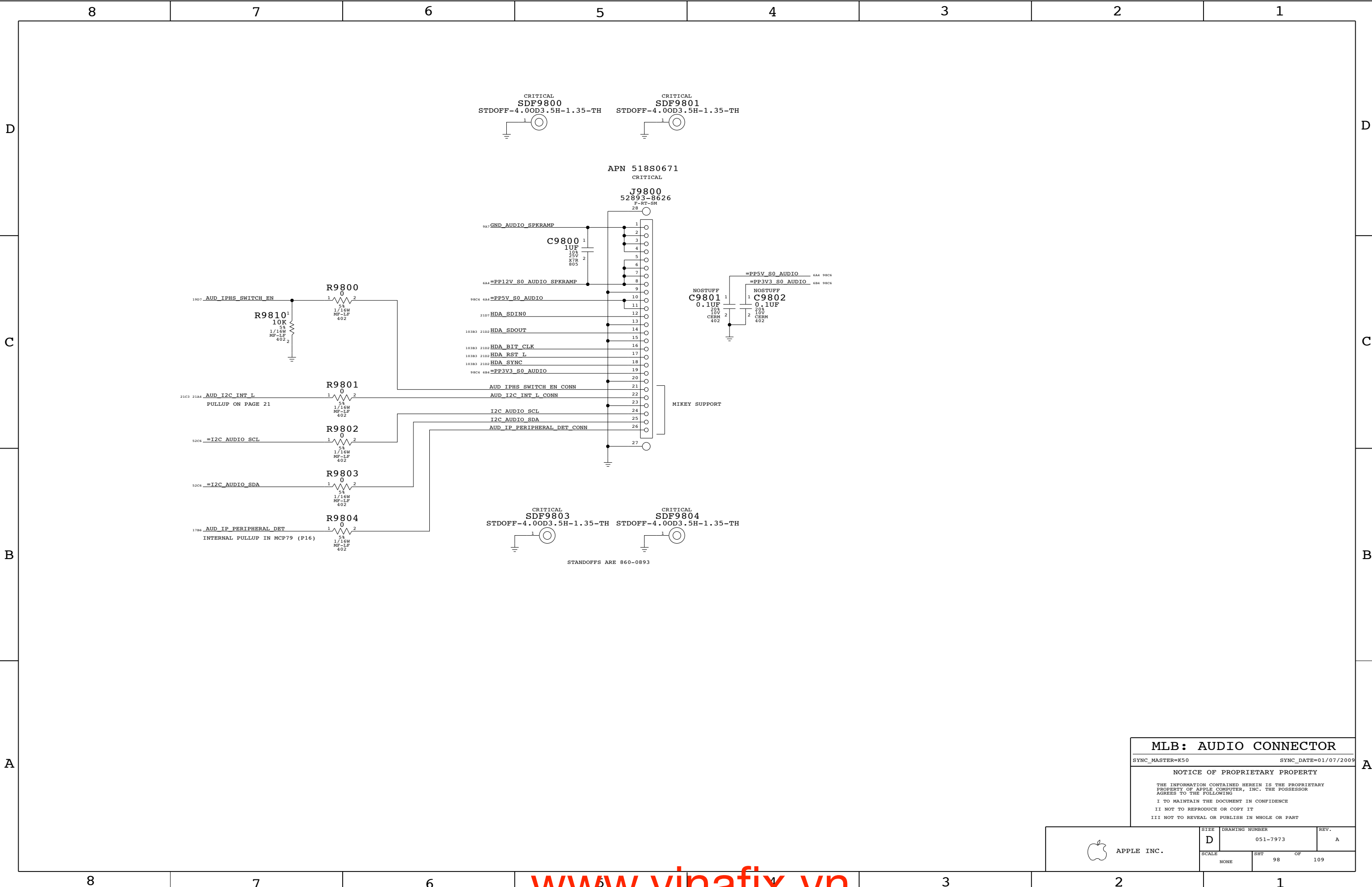
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**MLB: AUDIO CONNECTOR**

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FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=2x_DIELECTRIC	?
FSB_DSTB	*	=3x_DIELECTRIC	?
FSB_ADDR	*	=STANDARD	?
FSB_ADSTB	*	=2x_DIELECTRIC	?
FSB_1X	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_DSTB	TOP,BOTTOM	=5x_DIELECTRIC	?
FSB_ADDR	TOP,BOTTOM	=3x_DIELECTRIC	?
FSB_ADSTB	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_1X	TOP,BOTTOM	=3x_DIELECTRIC	?

All 4x/2x/1x FSB signals with impedance requirements are 50-ohm single-ended.

FSB 4X signals / groups shown in signal table on right.  
Signals within each 4x group should be matched within 5 ps of strobe.  
DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to +/- 300 ps.  
Spacing is 2x dielectric between DATA#, DINV# signals, with 3x dielectric spacing to the DSTB#s.  
DSTB# complementary pairs are spaced normally and are NOT routed as differential pairs.

FSB 2X signals / groups shown in signal table on right.  
Signals within each 2x group should be matched within 20 ps. ADTSB#s should be matched +/- 300 ps.  
Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADSTB#.

FSB 1X signals shown in signal table on right.  
Signals within each 1x group should be matched to CPU clock, +0/-1000 mils.

Design Guide recommends each strobe/signal group is routed on the same layer.  
Intel Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: MCP79 Interface DG (DG-03328-001\_v01), Section 2.2  
SOURCE: Santa Rosa Platform DG, Rev 1.5 (#22294), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	0.175 MM	0.175 MM

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	0.2 MM	?
CPU_COMP	*	0.6 MM	?
CPU_GTLREF	*	0.6 MM	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	0.6 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?

SR DG recommends at least 25 mils, >50 mils preferred

MOST CPU SIGNALS WITH IMPEDANCE REQUIREMENTS ARE 50-OHM SINGLE-ENDED.  
Some signals require 27.4-ohm single-ended impedance.

SOURCE: MCP79 Interface DG (DG-03328-001\_v01), Section 2.2  
SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

MCP FSB COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_FSB_COMP	*	0.2 MM	?

SOURCE: MCP79 Interface DG (DG-03328-001\_v01), Section 2.2.4

FSB Clock Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001\_v01), Section 2.2.5

FSB 2X Signals

FSB 4X Signal Groups

FSB 1X Signals

CPU / FSB Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
FSB_DATA_GROUP0_PP	FSB_50S	FSB_DATA	FSB D L<0>	707 708 1004 1403
FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB D L<15..1>	1004 1403
FSB_DATA_GROUP0_PP	FSB_50S	FSB_DATA	FSB DINV L<0>	707 708 1004 1406
FSB_DSTB_PP	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<0>	707 708 1004 1406
FSB_DATA_GROUP1_PP	FSB_50S	FSB_DATA	FSB DSTB L N<0>	1004 1406
FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB D L<16>	707 708 1004 1403
FSB_DATA_GROUP1_PP	FSB_50S	FSB_DATA	FSB D L<31..17>	1084 1004 1403 1403
FSB_DSTB1_PP	FSB_DSTB_50S	FSB_DSTB	FSB DINV L<1>	1084 1406
FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB DSTB L P<1>	707 708 1084 1406
FSB_DATA_GROUP2_PP	FSB_50S	FSB_DATA	FSB DSTB L N<1>	1084 1406
FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB D L<40..32>	1002 1403
FSB_DATA_GROUP2_PP	FSB_50S	FSB_DATA	FSB D L<41>	707 708 1002 1403
FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB D L<47..42>	1002 1483 1403
FSB_DATA_GROUP2_PP	FSB_50S	FSB_DATA	FSB DINV L<2>	707 708 1002 1406
FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<2>	1002 1406
FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB DSTB L N<2>	707 708 1002 1406
FSB_DATA_GROUP3_PP	FSB_50S	FSB_DATA	FSB D L<58..48>	1082 1002 1483
FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB D L<59>	707 708 1082 1483
FSB_DATA_GROUP3_PP	FSB_50S	FSB_DATA	FSB D L<63..60>	1082 1483
FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB DINV L<3>	707 708 1082 1406
FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB DSTB L P<3>	1082 1406
FSB_ADDR_GROUP0_PP	FSB_50S	FSB_ADDR	FSB DSTB L N<3>	707 708 1082 1406
FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB A L<5..3>	1008 1406
FSB_ADDR_GROUP0_PP	FSB_50S	FSB_ADDR	FSB A L<6>	707 708 1008 1406
FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB A L<16..7>	1008 1406 1406
FSB_ADSTB_PP	FSB_50S	FSB_ADSTB	FSB REQ L<4..0>	707 708 1008 1486
FSB_ADDR_GROUP1	FSB_50S	FSB_ADDR	FSB ADSTB L<0>	707 708 1008 1486
FSB_ADDR_GROUP1_PP	FSB_50S	FSB_ADDR	FSB A L<26..17>	1008 1008 1406
FSB_ADDR_GROUP1	FSB_50S	FSB_ADDR	FSB A L<27>	707 708 1008 1406
FSB_ADDR_GROUP1	FSB_50S	FSB_ADDR	FSB A L<35..28>	1008 1406
FSB_ADSTB1_PP	FSB_50S	FSB_ADSTB	FSB ADSTB L<1>	707 708 1008 1486
FSB_1X	FSB_50S	FSB_1X	FSB ADS L	1006 1486
FSB_BREQ0_L_PP	FSB_50S	FSB_1X	FSB BREQ0 L	707 1006 1486 2303
FSB_1X_PP	FSB_50S	FSB_1X	FSB BREQ1 L	1486
FSB_1X_PP	FSB_50S	FSB_1X	FSB BNR L	707 1006 1486
FSB_1X_PP	FSB_50S	FSB_1X	FSB BPRI L	1006 1483
FSB_1X	FSB_50S	FSB_1X	FSB DBSY L	707 1006 1486
FSB_1X	FSB_50S	FSB_1X	FSB DEFER L	1006 1483
FSB_1X_PP	FSB_50S	FSB_1X	FSB DRDY L	1006 1486
FSB_1X_PP	FSB_50S	FSB_1X	FSB HIT L	707 1006 1486
FSB_1X_PP	FSB_50S	FSB_1X	FSB HITM L	707 1006 1486
FSB_1X_PP	FSB_50S	FSB_1X	FSB LOCK L	707 1006 1486
FSB_CPURST_L	FSB_50S	FSB_1X	FSB CPURST L	14A3 23C3 1006 13C2
FSB_1X	FSB_50S	FSB_1X	FSB RS L<2..0>	14A6 1006
FSB_1X	FSB_50S	FSB_1X	FSB TRDY L	1486 1006
CPU_ASYNC_PP	CPU_50S	CPU_AGTL	CPU A20M L	708 14A3 1008
MCP_BSEL	CPU_50S	CPU_AGTL	MCP BSEL<2..0>	23B6 23C6
CPU_ASYNC_R	CPU_50S	CPU_8MIL	CPU FERR L	1008 1487
CPU_ASYNC_PP	CPU_50S	CPU_AGTL	CPU IGNE L	708 14A3 1008
CPU_ASYNC_PP	CPU_50S	CPU_AGTL	CPU INIT L	708 14A3 1006
CPU_ASYNC_PP	CPU_50S	CPU_AGTL	CPU INTR	708 14A3 1008
CPU_ASYNC_PP	CPU_50S	CPU_AGTL	CPU NM1	708 14A3 1088
CPU_PROCHOT	CPU_50S	CPU_AGTL	CPU PROCHOT L	1005 1486 50B3
CPU_PWRGD	CPU_50S	CPU_AGTL	CPU PWRGD	14A3 784 1082 1307
CPU_ASYNC_PP	CPU_50S	CPU_AGTL	CPU SMI L	708 14A3 1088
CPU_ASYNC_PP	CPU_50S	CPU_AGTL	CPU STPCLK L	708 14A3 1008
PM_THRMTRIP_L	CPU_50S	CPU_8MIL	PM THRMTRIP L	1006 50B1 1487
FSB_CPUSLP_L	CPU_50S	CPU_AGTL	FSB CPUSLP L	14A3 1082
CPU_50S	CPU_50S	CPU_AGTL	CPU DFLSLP L	14A3 1082
CPU_50S	CPU_50S	CPU_AGTL	CPU DPRSTP L	14A3 1082 71C7
CPU_50S	CPU_50S	CPU_AGTL	FSB DPWR L	707 14A3 1082
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_BCLK_VML_COMP_VDD	14A6
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_BCLK_VML_COMP_GND	14A6
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP CPU_COMP_VCC	14A6
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP CPU_COMP_GND	14A6
CLK_FSB_CPU_PP	CLK_FSB_100D	CLK_FSB	FSB CLK CPU P	708 1483 1086
CLK_FSB_ITP	CLK_FSB_100D	CLK_FSB	FSB CLK CPU N	708 1483 783 1086
CLK_FSB_ITP	CLK_FSB_100D	CLK_FSB	FSB CLK ITP P	1483 784 1303
CLK_FSB_MCP	CLK_FSB_100D	CLK_FSB	FSB CLK ITP N	1483 784 1303
CLK_FSB_MCP	CLK_FSB_100D	CLK_FSB	FSB CLK MCP P	14A4
CLK_FSB_MCP	CLK_FSB_100D	CLK_FSB	FSB CLK MCP N	14A4
CPU_IERR_L	CPU_50S	CPU_AGTL	CPU IERR L	1006
PM DPRSLPVR	CPU_50S	CPU_AGTL	PM DPRSLPVR	21C7 71C8
(See above)	CPU_50S	CPU_AGTL	IMVP DPRSLPVR	71C7
CPU_GTLREF	CPU_50S	CPU_GTLREF	CPU GTLREF	29B2 10B4
CPU_COMP	CPU_50S	CPU_COMP	CPU COMP<3>	10B3
CPU_COMP	CPU_27P4S	CPU_COMP	CPU COMP<2>	10B3
CPU_COMP	CPU_50S	CPU_COMP	CPU COMP<1>	10B3
CPU_COMP	CPU_27P4S	CPU_COMP	CPU COMP<0>	10B3
XDP_TDI_K50	CPU_50S	CPU_ITP	XDP TDI	13B3 784 1086 1006
XDP_TDO_K50	CPU_50S	CPU_ITP	XDP TDO	1006 784 1086 13B3
XDP_TMS_K50	CPU_50S	CPU_ITP	XDP TMS	13B3 784 1086 1006
XDP_TCK_K50	CPU_50S	CPU_ITP	XDP TCK	13B6 784 10A6 1006
XDP_TRST_L_K50	CPU_50S	CPU_ITP	XDP TRST L	13B3 784 10A6 1006
XDP_BPM_L	CPU_50S	CPU_ITP	XDP BPM L<4..0>	1006 1306 784
XDP_BPM_L5	CPU_50S	CPU_ITP	XDP BPM L<5>	1005 1306 784
(FSB_CPURST_L)	CPU_50S	CPU_ITP	XDP CPURST L	7A4 1304
CPU_50S	CPU_8MIL	IMVP6_VID<6..0>	12C1 71C7	
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE P	11B5 71A3
(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE N	11A5 71A3
CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_P	71A5	
CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_N	71A5	

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CPU/FSB Constraints

SYNC\_MASTER=K50

SYNC\_DATE=01/07/2009

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